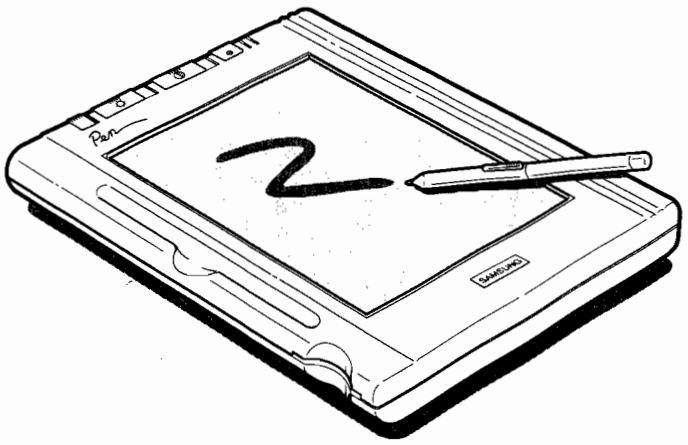
Service Manual

Pen MASTER 386L/20

V24984



SAMSUNG

Pen Computer System

Service Manual

Federal Communications Commision (FCC) Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and receiver.

Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

Consult the dealer or an experienced radio/T.V. technician for help.

NOTE

Peripherals used in conjunction with this equipment must have shielded interface cables only. A shielded power cable must also be used to connect this equipment. Use of non-shielded cables may result in interference to radio and TV reception, and may void the user's right to operate the equipment. The AC adapter adjusts itself to a wide range of AC voltage inputs (100 to 250 volts); therefore, you can use it anywhere in the world.

Canadian Department of Communications (CDC) Statement

This device does not exceed the Class B limits for radion noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Contents

About this Manual

This Service Manual provides specifications, removal and replacement procedures, optional equipment installation procedures, instructions for using the system diagnostics, and a description of the principles of operation of the equipment. It is intended for use by trained service personnel, and does not provide instruction on basic service knowledge or techniques such as soldering and electronic theory.

Manual Organization

The information in this manual is organized as follows:

Chapter 1 System Description — Provides a general product overview, lists specifications, and illustrates the main components and all connectors.

Chapter 2 Removal and Replacement Procedures — Step-by-step procedures for product disassembly and assembly.

Chapter 3 Optional Equipment — Lists the available optional equipment and includes installation instructions.

Chapter 4 Diagnostics — Provides instructions for the use of the system diagnostics.

Chapter 5 Principles of Operation — Describes the theory of operation.

Appendix A Schematics — Provides a complete set of system schematics to be used in troubleshooting and in conjunction with Chapter 5.

Appendix B Parts List — Lists the part numbers for all field-replaceable parts.

Appendix C Reference Material — Includes the following reference materials: IRQ Map, Memory Map, Acronym List, and a Units of Measure list.

Related Manuals

The following publications contain related information:

Internal Modem User's Guide

MS-DOS User's Guide and Reference

Manuals for Microsoft Windows for Pen Computing

Manuals for PenPoint

Manuals for PenDOS

Instruction sheets for the Automotive Power Adapter, External Charger, and External Diskette Drive

User's Guides for the Pen Computer System

1. System Description

1 System Description

Contents

Figures

Tables

General Description

This service manual covers the pen computer system shown in Figure 1-1. The basic computer system is comprised of four units, the computer itself, the internal (removable) battery pack, the external AC adapter, and the pen. Optional equipment, such as 48 KB cache-memory expansion, 4 or 16 MB memory-expansion boards, 80 and 120 MB hard disk drives (in place of the standard 60 MB drive), an internal fax/data modem, an external 1.44 MB diskette drive, FLASH-ROM and SRAM memory cards, an automotive power adapter, an external battery charger, and extra battery packs are available separately.

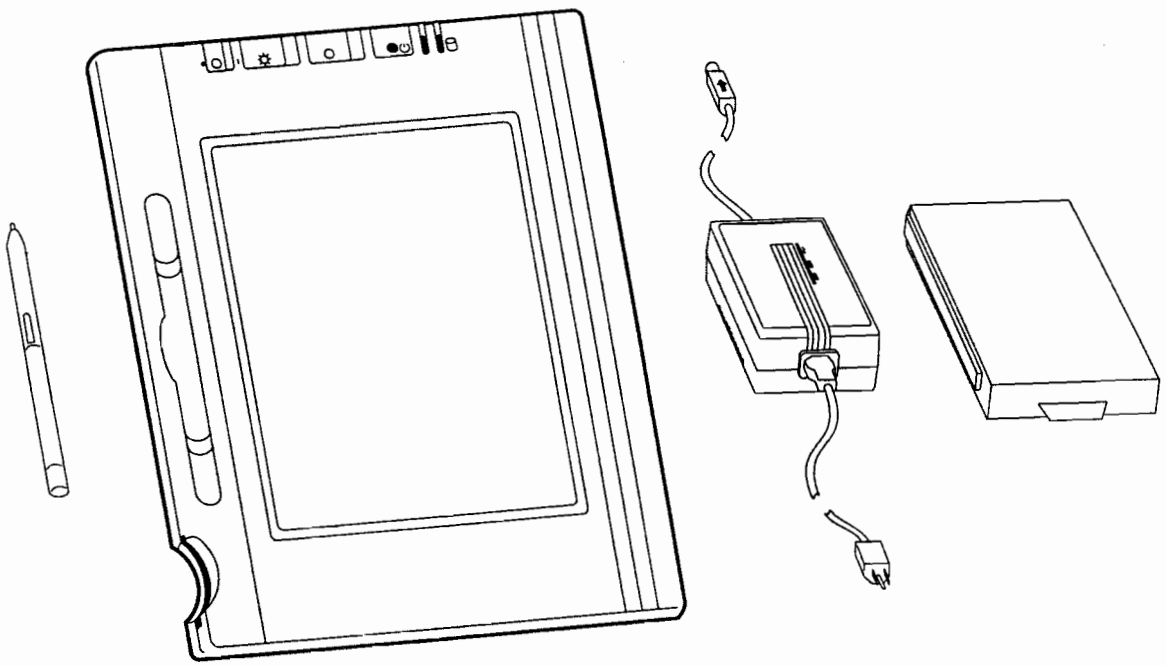


Figure 1-1. Pen Computer System

This system uses the Intel 80386SL microprocessor, the Intel 82360SL integrated ISA-peripheral and power-management controller, an 82077AA floppy disk controller, and the Western Digital WD90C22 VGA display controller, and includes 4 MB of DRAM and 16 KB of cache SRAM in its standard configuration. The built-in LCD display is integrated with the digitizer that converts input from the cordless pen to digital data. Pen activity is sensed by the digitizer's electromagnetic interface. A PCMCIA/JEIDA-compliant memory-card receptacle that supports SRAM and FLASH-ROM memory cards is built-in on the system board. The system's internal hardware configuration is shown in Figure 1-2, and specification for these components are provided in Table 1-2.

Standard peripheral devices are supported through the externally accessible serial and parallel ports. Other externally-accesible ports allow the user to connect AT- or PS/2-compatible keyboards (with 6-pin mini-DIN connectors), an analog VGA monitor, or the optional 1.44 MB external diskette drive.

The externally accessible power-input connector can be used with the AC adapter provided with the unit or with the optional automotive power adapter. DC power provide by either adapter is converted to the proper operating voltages by the internal DC/DC power supply.

Numerous power-conservation features are provided. The SETUP program included in the system BIOS ROM provides options that allow the user to select and configure the power-management timers. The system can be placed in Suspend mode at any time by pressing the Suspend/Resume switch with the pen tip. When implemented, the power-conservation features significantly extend the 2-hour operating time normally provided by a fully charged battery pack.

Table 1-1. System Specifications

Item	Description
CPU	Intel 80386SL
System clock	20 MHz
RAM	4 MB DRAM standard, expandable to 8 or 20 MB
Memory cache	16 KB standard, expandable to 64 KB
Embedded interfaces	IDE hard disk drive, pen digitizer, modem, VGA monitor, keyboard, serial, parallel, memory card
Embedded controllers	Diskette drive, VGA monitor, keyboard
Built-in display	10-inch (diagonal), transmissive CCFT, edge-lit LCD; maximum resolution of 640 X 480 in 32 shades of gray; 10:1 contrast ratio
Memory-card interface	Accepts SRAM and FLASH-ROM memory cards (PCMCIA 1.0/JEIDA 3.0)
BIOS	Phoenix LAP386SL system BIOS (version 1.1) and Chips & Technologies VGA BIOS in one 128 KB EPROM
Internal DC/DC power supply	Input: + 17/+ 17.5 VDC Outputs: + 5VDC, – 5 VDC, + 12VDC, + 30 VDC, BATT+ (see page 1-34)
External power supply	AC Adapter: 100 – 250 VAC input (auto-sensed), 17.5 VDC @ 1.3 A (1.5 A max.) output Auto Adapter: 11 – 16 VDC input, 17 VDC output @ 1.7 A (max.)
Battery pack	Removable, internal, 20.4 Whr NiCd
Drive mount	One internal mount for 2½-inch IDE hard disk drive
Drives	60 MB IDE hard disk drive (standard) 80 and 120 MB IDE hard disk drives (optional*) 1.44 MB, 3½-inch diskette drive (optional**)

* Single drive mount for 60, 80, or 120 MB IDE hard disk drive
** Diskette drive does not mount in unit — external diskette drive connects at FDD port

Hardware Configuration and Specifications

System Level

Figure 1-2 shows the standard and optional internal system components and subassemblies. Table 1-2 lists the main subassemblies and describes their main features. These subassemblies are described in greater detail in the next section.

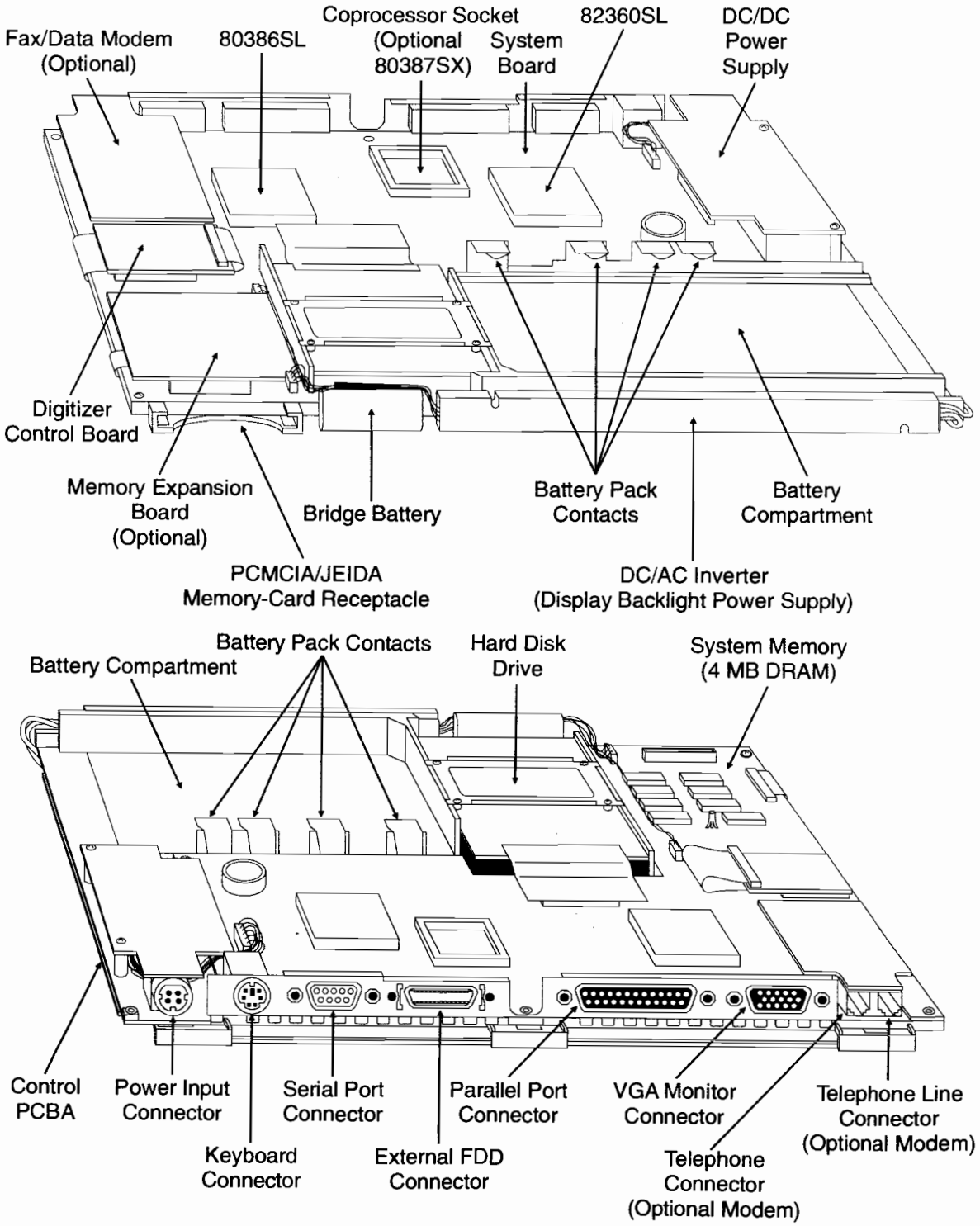


Figure 1-2. Hardware Configuration

Table 1-2. Hardware Configuration (System Level)

Item	Main Features
System board	4 MB DRAM; BIOS ROM; Intel 80386SL & 82360SL; memory cache; IDE, modem,serial, parallel, and keyboard interfaces; memory-card interface and receptacle; FDD controller; VGA display controller
System memory	4 MB DRAM on system board, expandable to 8 or 20 MB using optional 4 or 16 MB memory expansion boards
Memory-cache	16 KB or 64 KB (factory option) SRAM on system board; cache controller included in 82360SL
Internal DC/DC power supply	Input: + 17/+ 17.5 VDC Outputs: + 5VDC, – 5 VDC, + 12VDC, + 30 VDC, BATT+ (see page 1-34)
Hard disk drive	2½-inch; 60, 80, or 120 MB IDE (80 and 120 MB drives optional)
Bridge battery	Non-removable, internal, 0.36 Whr NiCd
Memory-card receptacle	Compatible with PCMCIA (ver. 1.0) and JEIDA (ver 3.0) specifications; Supports SRAM and FLASH-ROM memory cards
Serial port	Compatible with IBM implementation of RS-232-C specification; male DB-9 connector
Parallel port	Compatible with IBM implementation of Centronics parallel printer interface; female DB-25 connector
Keyboard port	Accepts AT- or PS/2-compatible keyboards with 6-pin mini-DIN connectors; female, 6-pin, mini-DIN connector
VGA monitor port	Standard analog VGA output (640 x 480 resolution in 16 colors); female DB-15 connector
Diskette drive port	Proprietary interface for optional external 3½-inch, 1.44 MB diskette drive; female, 26-pin, D-subminiature connector
Modem interface	Proprietary interface for optional internal data/fax modem (modem uses standard RJ-11 telephone input/output connectors

Subassembly Level

The following major system subassemblies are described in this section:

- Case
- System board
- Mass storage devices
- Internal power supply
- External power supplies
- Display
- Digitizer (pen interface)

The description of each subassembly includes a table of specifications and, where applicable, illustrations and pin assignment tables of associated connectors.

Case

The case is comprised of five pieces: the front and back halves of the clamshell, and the three connector covers, as shown in Figure 1-3. The case specifications are listed in Table 1-3.

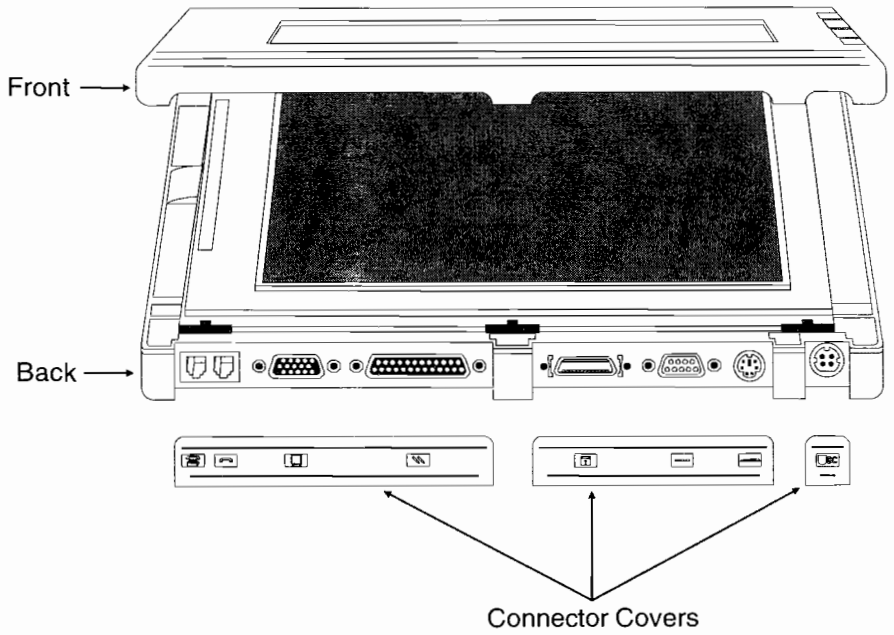


Figure 1-3. Case Components

Table 1-3. Case Specifications

Category	Description
Design	Notepad (clamshell)
Construction	Clamshell: molded PC/ABS plastic (polycarbonate/acrylonitrile butadiene styerene) Connector covers: molded thermoplastic polyurethane elastomer
Dimensions Width Height Depth	 11.5 inches (292.1 mm) 9.3 inches (236.2 mm) 1.5 inches (38.1 mm)
Weight (including battery pack)	5.40 lb. (2.432 kg)

System Board

All components and circuitry that support common ISA (AT-compatible) functions are on the system board, which also includes the following additional peripheral support functions:

- Diskette drive controller
- IDE hard disk drive interface
- Serial and parallel ports
- Keyboard port
- Display controller (standard VGA)

Figure 1-4 shows the following system-board components:

- Intel 80386SL microprocessor (CPU and memory-controller subsystem)
- Intel 82360SL ISA subsystem controller (with integrated system power management)
- Western Digital WD90C20 VGA controller
- 82077AA FDD controller
- 4 MB DRAM (8 – KM44C1000ALJ-8)
- 256 KB video RAM (2 – 511664-8)
- Numeric coprocessor socket (for Intel 80387SX)
- External connectors for: keyboard, VGA monitor, external FDD, parallel port, and serial port

Table 1-4 lists and describes the major functions on the system board. Figure 1-5, on page 1-13, shows the locations and functions of all main-system-board connectors.

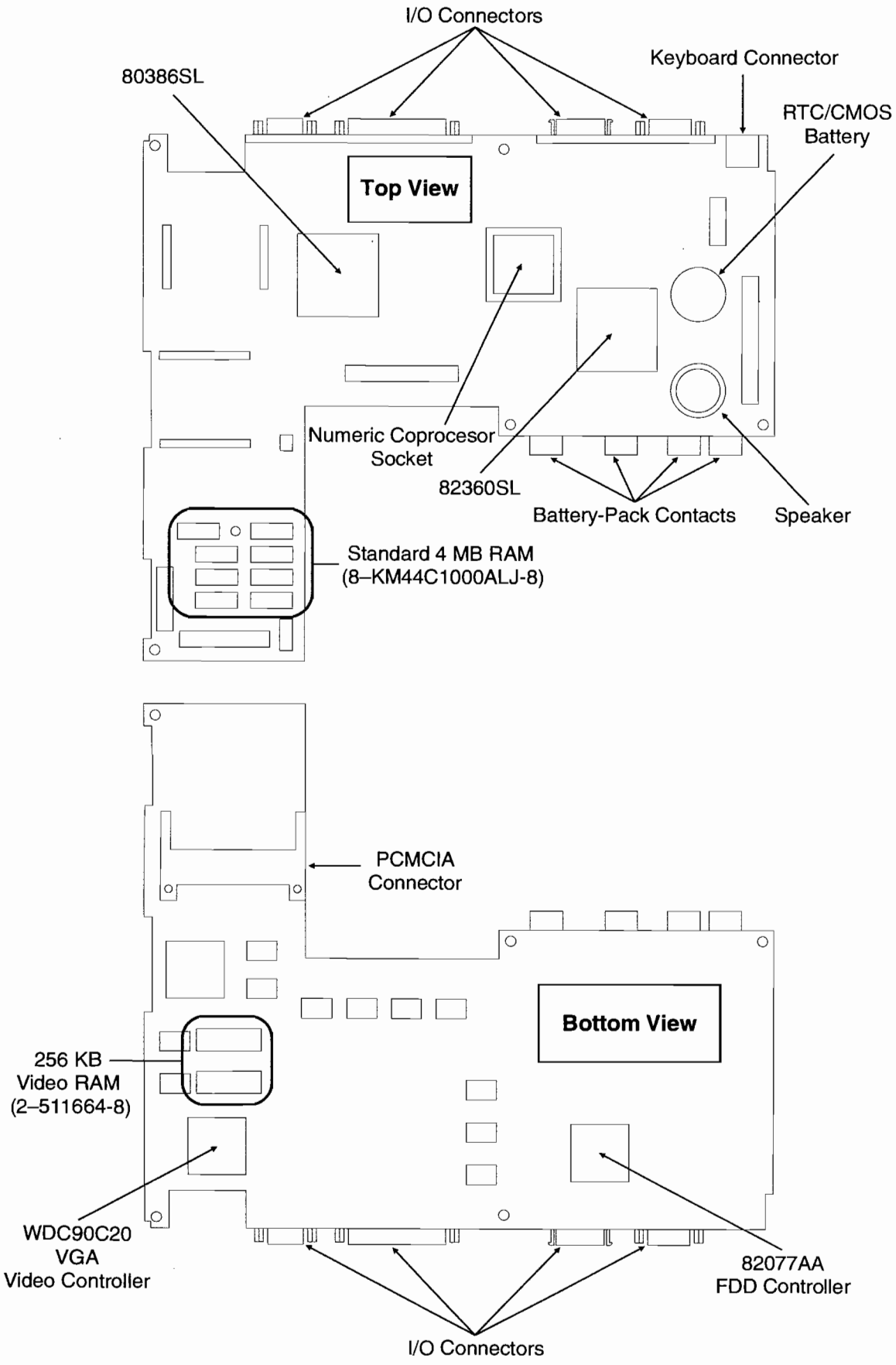


Figure 1-4. System Board Components

Table 1-4. Major System Board Functions

Item	Description
Microprocessor	20 MHz Intel 80386SL (includes on-chip memory-controller subsystem)
Numeric coprocessor	20 MHz Intel 80387SX (optional)
DRAM	4 MB on eight 512 KB (1Mb x 4), fast page mode, KM44C1000ALJ-8 (20-pin SOJ)
DRAM expansion	Expandable to 8 or 20 MB using 4 or 16 MB proprietary memory-expansion boards
Real-time clock	146818-compatible real-time clock/calendar with 128 bytes battery-backed CMOS RAM (part of 82360SL)
Keyboard controller	8042-compatible (part of 82360SL)
FDD controller	Intel 82077AA
Serial/Parallel port drivers	16450-compatible serial port driver; 8-bit bi-directional parallel port driver (part of 82360SL)
Memory-card interface	PCMCIA version 1.0 (JEIDA 3.0)-compatible; accepts SRAM and FLASH-ROM memory cards
VGA controller	Western Digital WD90C20
VGA RAMDAC	PS/2-compatible (part of WD90C20)

Integrated Peripheral Interfaces

Table 1-5 lists and describes the peripheral interface and control functions that are embedded on the system board. The locations of the connectors for these interfaces are shown in Figure 1-5.

Table 1-5. Integrated Peripheral Interfaces and Controllers

	Function	Connector Type
Peripheral interfaces	Serial port Parallel port Keyboard interface Pen-digitzer interface Modem	9-pin D-shell, male 25-pin D-shell, female 6-pin mini-DIN, female 2–14-pin female headers 2–10-pin female headers
Peripheral controllers	Diskette drive controller VGA monitor controller	26-pin mini-Centronics 15-pin D-shell, female

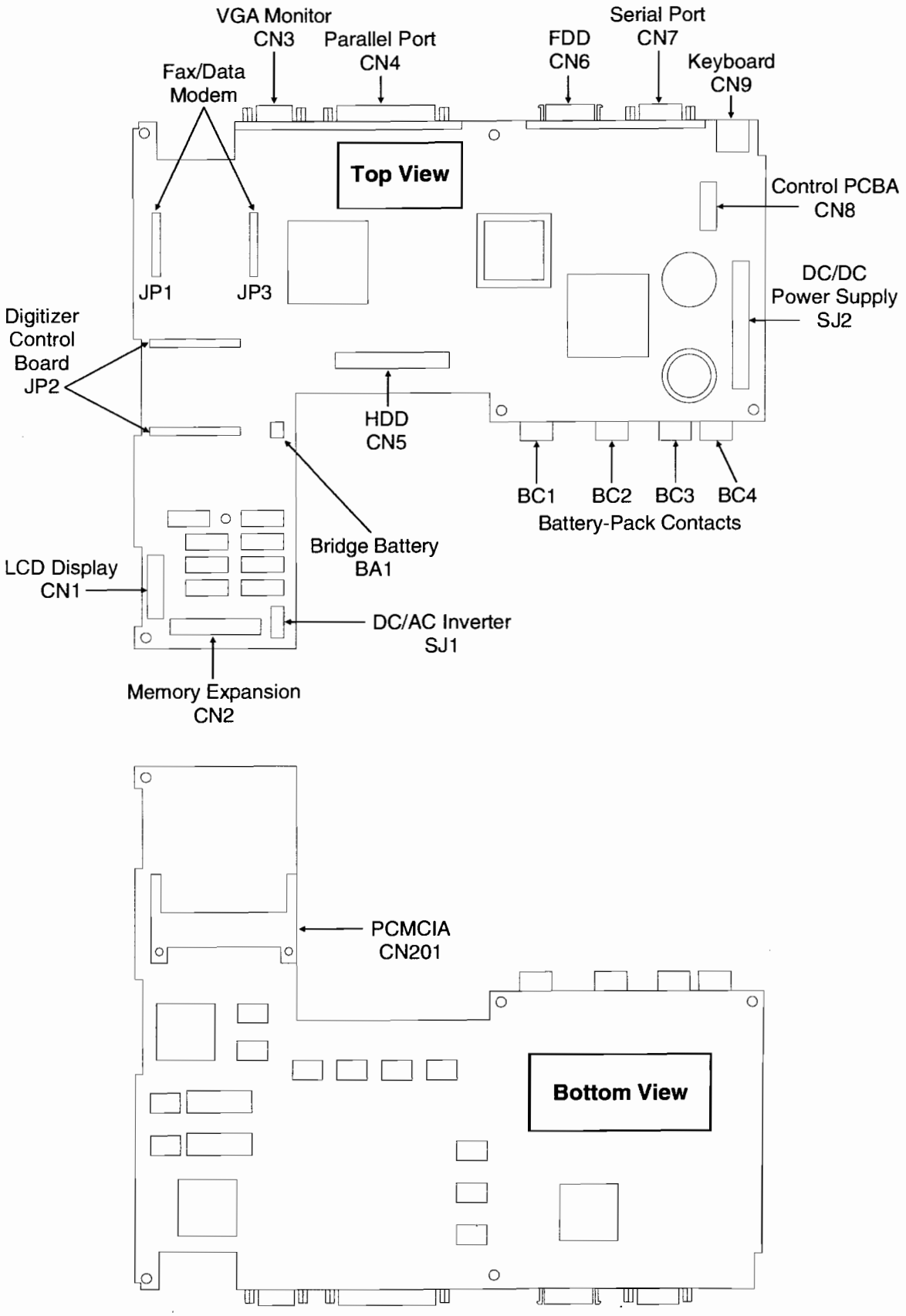


Figure 1-5. System Board Connector Locations

System Connectors

Figures 1-6 through 1-25 contain illustrations of each of the system's connectors shown in Figure 1-5. Tables 1-6 through 1-20 list the pin assignments for these connectors. Connectors on the hard disk drive, the internal power supply, the external power supply, the LCD display, and the digitizer are described with their respective components.

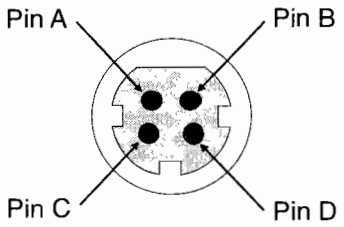


Figure 1-6. Internal Power Supply Input Connector

Table 1-6. Internal Power Supply Input Connector Pin Assignments

Pin *	Signal
A	VBATT
B	MODE
C	VMAIN
D	GND

* The pin designations in the table and illustration above (A, B, C, and D) are for illustration purposes only; these do not appear on the connector or the power supply.

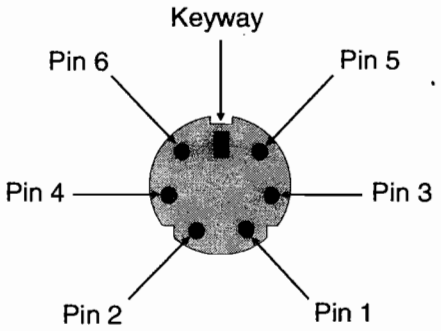


Figure 1-7. Keyboard Connector (CN9)

Table 1-7. Keyboard Connector Pin Assignments

Pin	Signal
1	Data
2	NC
3	GND
4	+ 5 V
5	CLK
6	NC

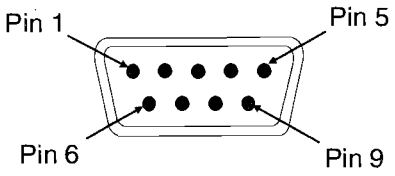


Figure 1-8. Serial Port Connector (CN7)

Table 1-8. Serial Port Connector Pin Assignments

Pin	Signal	Pin	Signal
1	DCDA	6	DSRA
2	RXDA	7	RTSA
3	TXDA	8	CTSA
4	DTRA	9	RIA
5	SGND		

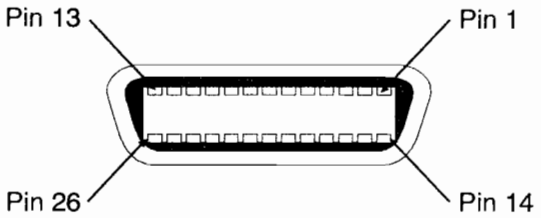


Figure 1-9. FDD Connector (CN6)

Table 1-9. FDD Connector Pin Assignments

Pin	Signal	Pin	Signal
1	+ 5VFD	14	BSTEP
2	BINDEX	15	GND
3	+ 5VFD	16	BWRDATA
4	BDS0	17	GND
5	+ 5VFD	18	BWGATE
6	BDSKCHG	19	GND
7	+ 5VFD	20	BTRK0
8	READY	21	GND
9	BDS1	22	BWP
10	BMOTORON	23	GND
11	BDENSEL#	24	RDDATA
12	BDIR	25	GND
13	GND	26	BHSEL

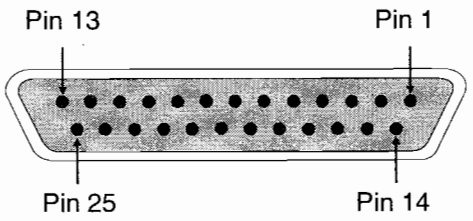


Figure 1-10. Parallel Port Connector (CN4)

Table 1-10. Parallel Port Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal
1	ALPTSTROBE#	10	ALPTACK#	19	PGND
2	ALPTD0	11	ALPTBUSY	20	PGND
3	ALPTD1	12	ALPTPE	21	PGND
4	ALPTD2	13	ALPTSLCT	22	PGND
5	ALPTD3	14	AFD#	23	PGND
6	ALPTD4	15	ALPTERROR#	24	PGND
7	ALPTD5	16	ALPTINIT#	25	PGND
8	ALPTD6	17	SLCTIN#		
9	ALPTD7	18	PGND		

Active low logic

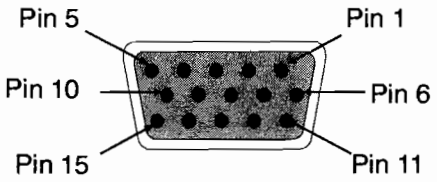


Figure 1-11. VGA Monitor Connector (CN3)

Table 1-11. VGA Monitor Connector Pin Assignments

Pin	Signal	Pin	Signal
1	VGARed	9	Unused
2	VGAGreen	10	Unused
3	VGABlue	11	Unused
4	Unused	12	Unused
5	CRTGND	13	VGAHSync
6	CRTGND	14	VGAVSync
7	CRTGND	15	Unused
8	CRTGND		

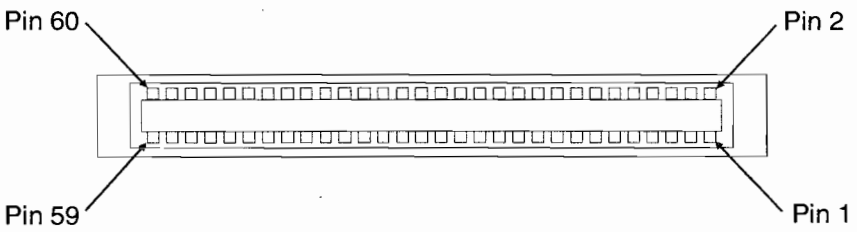


Figure 1-12. DC/DC Power Supply Connector (SJ2)

Table 1-12. DC/DC Power Supply Connector Pin Assignments

Pin	Singal	Pin	Signal	Pin	Signal	Pin	Signal
1	+ 30V	16	GND	31	Unused	46	BATT_TEMP
2	+ 30V	17	AC-DC_IN	32	Unused	47	POWER_DISABLE
3	Unused	18	GND	33	BATT–	48	BATT_RETURN
4	Unused	19	OUT	34	BATT–	49	+ 5VSYS
5	– 5V	20	GND	35	BATT–	50	+ 5VSYS
6	GND	21	IN	36	BATT–	51	+ 5VSYS
7	Unused	22	Unused	37	BATT–	52	+ 5VSYS
8	GND	23	BATT+	38	BATT–	53	+ 5VSYS
9	+ 12V	24	BATT+	39	BATT–	54	+ 5VSYS
10	GND	25	BATT+	40	BATT–	55	+ 5VSYS
11	+ 12V	26	BATT+	41	BATT_IN_USE#	56	+ 5VSYS
12	GND	27	BATT+	42	AMB_TEMP	57	+ 5VSYS
13	+ 12V	28	BATT+	43	BATTWARN#	58	+ 5VSYS
14	GND	29	BATT+	44	AMB_TEMP_RETURN	59	BATT_LOW_REAL#
15	AC-DC_IN	30	BATT+	45	XBATTLOW#	60	SYSPWROFF1

Active low logic

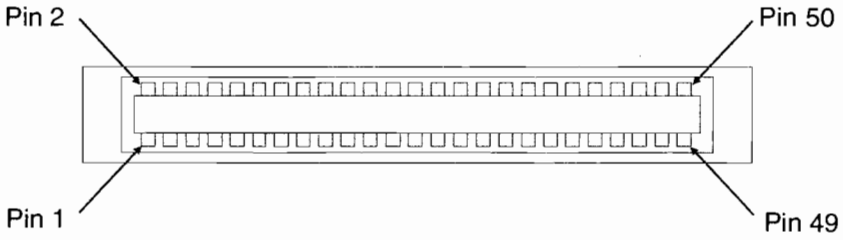


Figure 1-13. HDD Connector (CN5)

Table 1-13. HDD Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal
1	RESET#	18	HD12	35	+ 5VHD
2	HD8	19	GND	36	HIOR#
3	GND	20	HD3	37	+ 5VHD
4	HD7	21	GND	38	IOCHRDY
5	GND	22	HD13	39	+ 5VHD
6	HD9	23	GND	40	HIOCS16#
7	GND	24	HD2	41	+ 5VHD
8	HD6	25	GND	42	HIRQ14
9	GND	26	HD14	43	+ 5VHD
10	HD10	27	GND	44	Unused
11	GND	28	HD1	45	HDLED#
12	HD5	29	+ 5VHD	46	HSA1
13	GND	30	HD15	47	HDCS1#
14	HD11	31	+ 5VHD	48	HSA2
15	GND	32	HD0	49	HDCS0#
16	HD4	33	+ 5VHD	50	HSA0
17	GND	34	HIOW#		

Active low logic

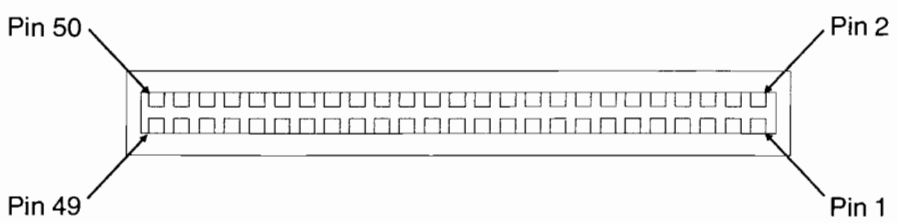


Figure 1-14. HDD Cable Connector (System Board End)

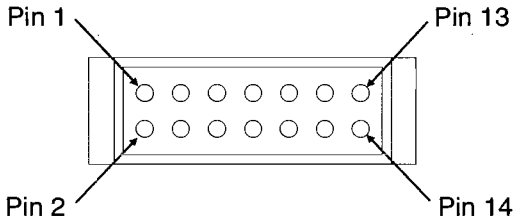


Figure 1-15. Control PCBA Connector (CN8)

Table 1-14. Control PCBA Connector (on System Board) Pin Assignments

Pin	Signal	Pin	Signal
1	HDLED	8	VLCD
2	BALOWLED	9	OUT
3	GND	10	IN
4	+ 5VSYS	11	SRBTN#
5	CCFTVR2	12	BATTLED
6	CCFTVR1	13	BRIDGEIN
7	VCONTRAST	14	BRIDGEOUT

Active low logic

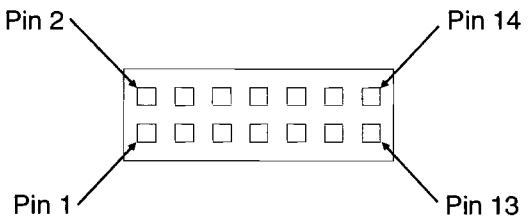


Figure 1-16. Control PCBA Cable Connector (System Board End)

Figure 1-17. Control PCBA Connector (on Control PCBA)

Table 1-15. Control PCBA Connector (on Control PCBA) Pin Assignments

Pin	Signal	Pin	Signal
1	HDLED	8	VLCD
2	BALOWLED	9	OUT
3	GND	10	IN
4	+ 5VSYS	11	SRBTN#
5	CCFTVR2	12	BATTLED
6	CCFTVR1	13	BRIDGEIN
7	VCONTRAST	14	BRIDGEOUT

Active low logic

Figure 1-18. Control PCBA Cable Connector
(Control PCBA End)

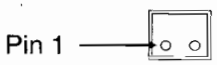


Figure 1-19. Bridge Battery Connector (BA1)

Table 1-16. Bridge Battery Connector Pin Assignments

Pin	Signal
1	BRIDGEIN
2	GND

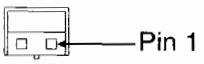


Figure 1-20. Bridge Battery Cable Connector

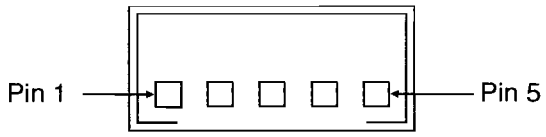


Figure 1-21. DC/AC Inverter Connector (SJ1)

Table 1-17. DC/AC Invertor Connector Pin Assignments

Pin	Signal
1	CCFTDCIN
2	GND CCFTRTN
3	CCFTON/OFF
4	CCFTVR1
5	CCFTVR2

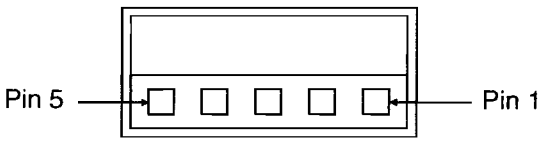


Figure 1-22. DC/AC Inverter Cable Connector (System Board End)

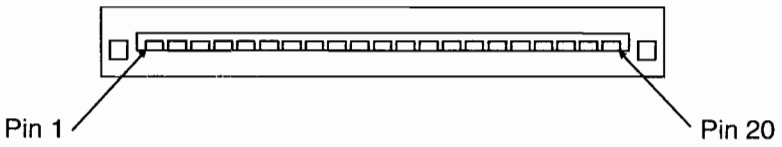


Figure 1-23. LCD Display Connector (CN1)

Table 1-18. LCD Display Connector Pin Assignments

Pin	Signal	Pin	Signal
1	VCONTRAST	11	UD0
2	VEE	12	UD1
3	GND	13	UD2
4	VDD	14	UD3
5	VLCD ON	15	LD0
6	Unused	16	LD1
7	LCDXSCLK	17	LD2
8	LCDLP	18	LD3
9	LCDFR	19	Unused
10	LCDFP	20	Unused

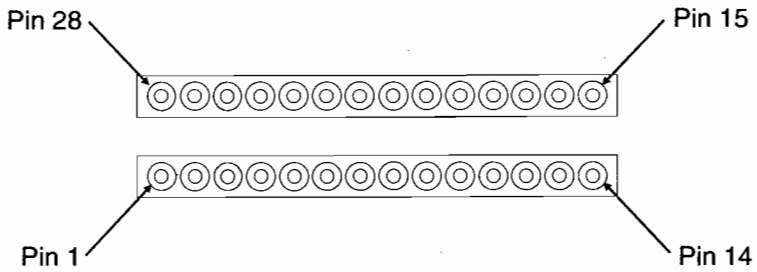


Figure 1-24. Digitizer Connector (JP2)

Table 1-19. Digitizer Connector Pin Assignments

Pin	Signal	Pin	Signal
1	– 5V	15	WD7
2	– 5V	16	WD6
3	Unused	17	WD5
4	Unused	18	WD4
5	GND	19	WD3
6	GND	20	WD2
7	GND	21	WD1
8	+ 5V	22	WD0
9	+ 5V	23	BIRQ10
10	REFRESH#	24	PWRRESET#
11	BDIGICS#	25	Unused
12	IOR#	26	Unused
13	IOW#	27	Unused
14	SA1	28	Unused

Active low logic

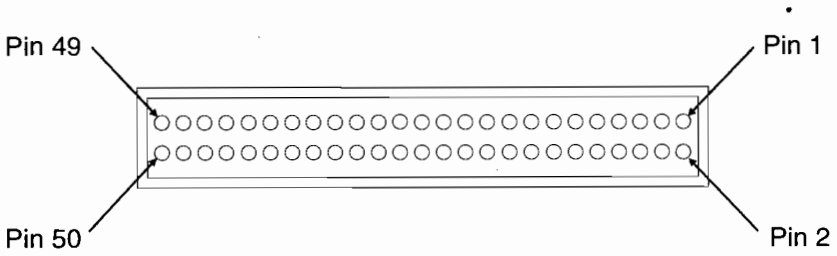


Figure 1-25. Memory Expansion Board Connector (CN2)

Table 1-20. Memory Expansion Board Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal
1	RAS#1	18	M7	35	MD8
2	WLE#	19	M3	36	MD7
3	RAS#2	20	PARL	37	MD9
4	WHE#	21	+ 5VMEM	38	MD12
5	RAS#3	22	GND	39	MD10
6	CASH#1	23	+ 5VMEM	40	MD13
7	CASL#1	24	GND	41	MD11
8	CASH#2	25	M8	42	MD14
9	CASL#2	26	M9	43	PARH
10	CASH#3	27	MD0	44	MD15
11	CASL#3	28	M10	45	+ 5VMEM
12	M4	29	MD1	46	GND
13	M0	30	MD4	47	+ 5VMEM
14	M5	31	MD2	48	GND
15	M1	32	MD5	49	GND
16	M6	33	MD3	50	GND
17	M2	34	MD6		

Active low logic

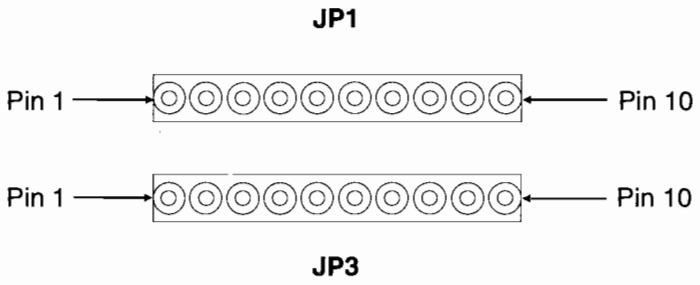


Figure 1-26. Modem Connector (JP1 and JP3)

Table 1-21. Modem Connector Pin Assignments

Connector JP1		Connector JP3	
Pin	**Signal**	**Pin**	**Signal**
1	COMBRXD	1	+ 5V
2	Unused	2	COMBDSR#
3	COMBDTR#	3	COMBDCD#
4	COMBCTS#	4	RESETDRV
5	COMBTXD	5	MODEM_AUDIO
6	COMBRTS#	6	GND
7	MODEM_RI#	7	GND
8	Unused	8	Unused
9	Unused	9	– 5V
10	Unused	10	Unused

Active low logic

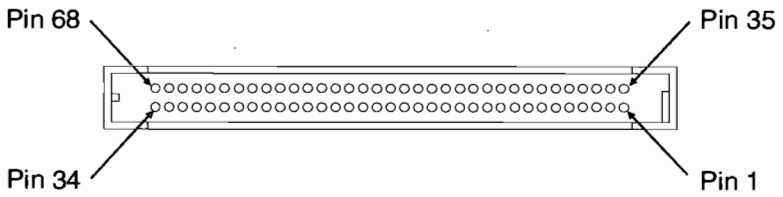


Figure 1-27. PCMCIA Connector (CN201)

Table 1-22. PCMCIA Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	18	FLASHVPP	35	GND	52	FLASHVPP
2	PCD3	19	PA16	36	CD1#	53	PA22
3	PCD4	20	PA15	37	PCD11	54	PA23
4	PCD5	21	PA12	38	PCD12	55	PA24
5	PCD6	22	PA7	39	PCD13	56	PA25
6	PCD7	23	PA6	40	PCD14	57	NC
7	CE1#	24	PA5	41	PCD15	58	NC
8	PA10	25	PA4	42	CE2#	59	NC
9	POE#	26	PA3	43	NC	60	NC
10	PA11	27	PA2	44	NC	61	REG#
11	PA9	28	PA1	45	NC	62	BVD2#
12	PA8	29	PA0	46	PA17	63	BVD1#
13	PA13	30	PCD0	47	PA18	64	PCD8
14	PA14	31	PCD1	48	PA19	65	PCD9
15	PWE#	32	PCD2	49	PA20	66	PCD10
16	RDY/BSY#	33	WP	50	PA21	67	CD2#
17	MCIAVCC	34	GND	51	MCIAVCC	68	GND

Active low logic

Hard Disk Drive

The specifications for the standard 60 MB and the optional 80 MB and 120 MB hard disk drives are provided in Table 1-23.

Table 1-23. Hard Disk Drive Specifications

	60 MB* **Conner CP2064/ Quantum Go•Drive 60**	**80 MB** **Quantum Go•Drive 80**	**120 MB** **Qua. tum Go•Drive 120**
Form factor	2½-inch	2½-inch	2½-inch
Outer dimensions (H × W × D)	.75 × 2.75 × 4.00 inches/ .61 × 2.76 × 4.00 inches	.75 × 2.76 × 4.00 inches	.75 × 2.76 × 4.00 inches
Weight	7 oz. (198.6 grams)/ 6.2 oz. (176 grams)	6.2 oz. (176 grams)	6.2 oz. (176 grams)
Media capacity (Formatted)	64 MB/63 MB	86.3 MB	126.6 MB
Interface	IDE	IDE	IDE
Data encoding method	RLL 1,7	RLL 1,7	RLL 1,7
Interleave	1:1	1:1	1:1
Platters	2/1	2	2
Data surfaces,heads	4,4/2,2	4,4	4,4
Tracks per data surface	823/1097	870	1097
Track capacity (formatted)	19,456 bytes/ 28,715 bytes	24,799 bytes	28,851 bytes
Bytes per block	512	512	512
Blocks per track	38/56	48	56
Blocks per drive	125,096/123,113	168,470	247,323
Recording density	39,222 fci/56,688 bpi	48,371 bpi	56,688 bpi
Data transfer rate (to/from media)	1.5 MB per second/ 2.66 MB per second	2.25 MB per second	2.66 MB per second
Rotational speed (rpm)	3486/3600	3600	3600
Seek times (ms)	19/19 (17 typical)	19	19 (17 typical)

* Separate specifications are given for the Conner and Quantum 60 MB drives only when they differ.

The HDD cable does not have straight-through connections. Table 1-24 provides the pin-to-pin wiring of the cable. Table 1-13 gives the pin assignments for the system-board end of the cable and Table 1-25 gives the pin assignments for the drive end of the cable.

Table 1-24. HDD Cable Pin-to-Pin Wiring

Pins on the Drive Side of the Cable	Pins on the System Board Side of the Cable	Pins on the Drive Side of the Cable	Pins on the System Board Side of the Cable
1	1	23	34
2	3	24	25
3	4	25	36
4	2	26	27
5	8	27	38
6	6	28	—
7	12	29	29
8	10	30	13
9	16	31	42
10	14	32	40
11	20	33	46
12	18	34	44
13	24	35	50
14	22	36	48
15	28	37	49
16	26	38	47
17	32	39	45
18	30	40	15
19	19	41	41
20	20	42	31
21	21	43	17
22	23	44	—

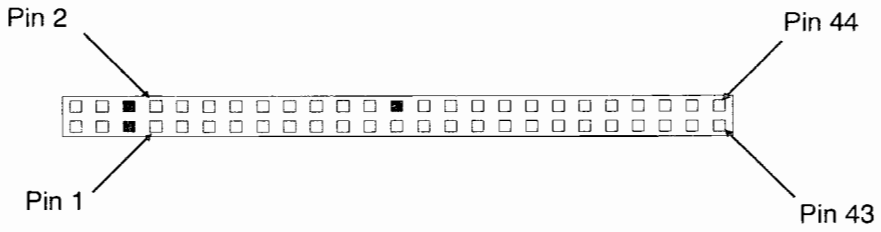


Figure 1-28. HDD Connector (on HDD)

Table 1-25. HDD Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal
1	RESET#	16	HD14	31	HIRQ14
2	GND	17	HD0	32	HIOCS16#
3	HD7	18	HD15	33	HSA1
4	HD8	19	GND	34	PDIAG#
5	HD6	20	Key	35	HSA0
6	HD9	21	Reserved	36	HSA2
7	HD5	22	GND	37	HDCS0#
8	HD10	23	HIOW#	38	HDCS1#
9	HD4	24	GND	39	HDLED#
10	HD11	25	HIOR#	40	GND
11	HD3	26	GND	41	+ 5VHD
12	HD12	27	IOCHRDY	42	+ 5VHD
13	HD2	28	Reserved	43	GND
14	HD13	29	Reserved	44	Reserved
15	HD1	30	GND		

Active low logic

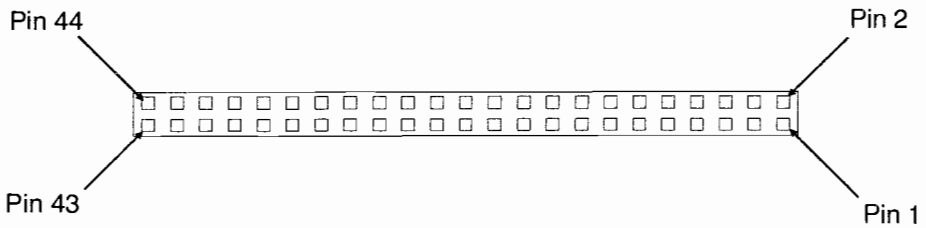


Figure 1-29. HDD Cable Connector (HDD End)

Internal Power Supply

Specifications for the internal DC/DC power supply, which is shown in Figure 1-30, are provided in Table 1-26.

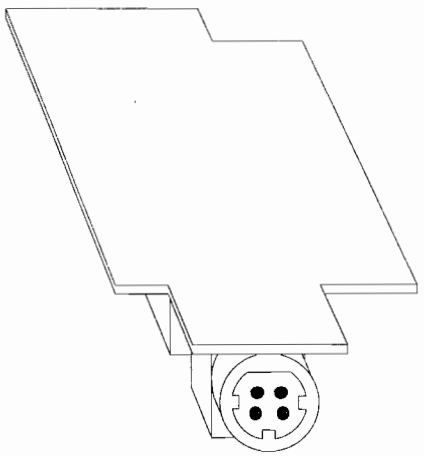


Figure 1-30. Internal (DC/DC) Power Supply

Table 1-26. Internal (DC/DC) Power Supply Specifications

Function	Description
Input voltage	16.4 – 17 VDC (from automotive or AC Adapter)
Output voltages	+ 5 VDC, – 5 VDC, + 12 VDC, + 30 VDC
Signals	BATT+ *
Input connector	4 pin mini-DIN
Battery pack	Removable 20.4 Whr NiCd battery pack

* BATT+ is bidirectional and is both a signal and an output. When the external power supply (AC adapter or automotive adapter) is connected and a battery pack is inserted, BATT+ is an output that is used to charge the battery pack. The voltage level (+ 10 to + 16.5 VDC) varies with the state of the battery. When no external power supply is connected, BATT+ is a DC voltage level input signal from the battery pack that indicates the current state of the battery pack.

The internal (DC/DC) power supply output and input connectors are shown in Figures 1-31 and 1-32, respectively. The pin assignments for these connectors are provided in Tables 1-27 and 1-28.

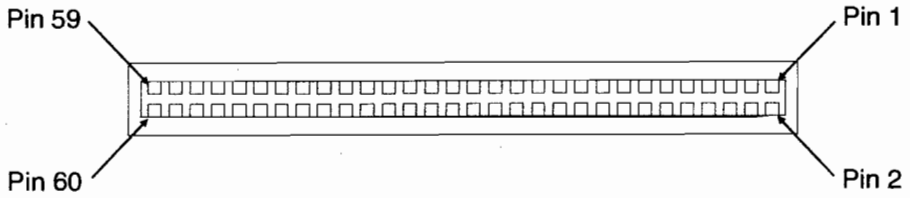


Figure 1-31. Internal (DC/DC) Power Supply Output Connector

Table 1-27. Internal (DC/DC) Power Supply Output Connector Pin Assignments

Pin	Singal	Pin	Signal	Pin	Signal	Pin	Signal
1	+ 30V	16	GND	31	Unused	46	BATT_TEMP
2	+ 30V	17	AC-DC_IN	32	Unused	47	POWER_DISABLE
3	Unused	18	GND	33	BATT–	48	BATT_RETURN
4	Unused	19	OUT	34	BATT–	49	+ 5VSYS
5	– 5V	20	GND	35	BATT–	50	+ 5VSYS
6	GND	21	IN	36	BATT–	51	+ 5VSYS
7	Unused	22	Unused	37	BATT–	52	+ 5VSYS
8	GND	23	BATT+	38	BATT–	53	+ 5VSYS
9	+ 12V	24	BATT+	39	BATT–	54	+ 5VSYS
10	GND	25	BATT+	40	BATT–	55	+ 5VSYS
11	+ 12V	26	BATT+	41	BATT_IN_USE#	56	+ 5VSYS
12	GND	27	BATT+	42	AMB_TEMP	57	+ 5VSYS
13	+ 12V	28	BATT+	43	BATTWARN#	58	+ 5VSYS
14	GND	29	BATT+	44	AMB_TEMP_RETURN	59	BATT_LOW_REAL#
15	AC-DC_IN	30	BATT+	45	XBATTLOW#	60	SYSPWROFF1

Active low logic

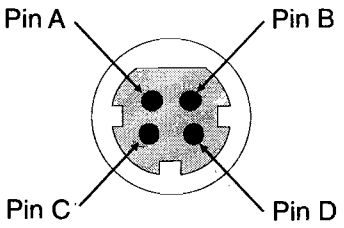


Figure 1-32. Internal (DC/DC) Power Supply Input Connector

Table 1-28. Internal (DC/DC) Power Supply Input Connector Pin Assignments

Pin *	Signal
A	VBATT
B	MODE
C	VMAIN
D	GND

* The pin designations in the table and illustration above (A, B, C, and D) are for illustration purposes only; these do not appear on the connector or the power supply.

External Power Supply

Specifications for the external power supply (AC adapter), which is shown in Figure 1-33, are provided in Table 1-29.

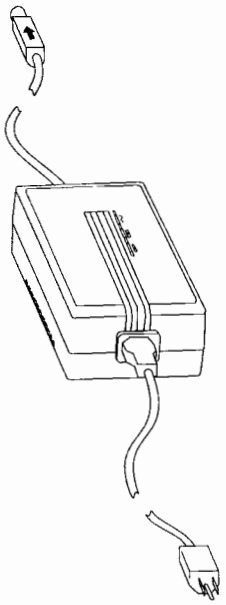


Figure 1-33. External Power Supply (AC Adapter)

Table 1-29. External Power Supply (AC Adapter) Specifications

Function	Description
Input voltage	99 – 121 VAC, 216 – 264 VAC
Input frequency	47 – 63 Hz
Input sensing	Automatic
Output	16.4 – 17 VDC

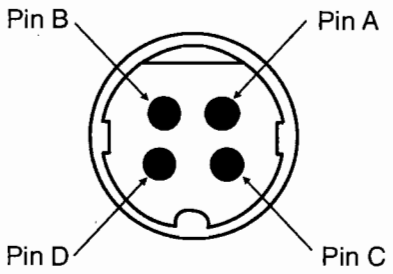


Figure 1-34. External Power Supply (AC Adapter) Output Cable Connector

Table 1-30. External Power Supply (AC Adapter) Output Connector Pin Assignments

Pin *	Signal
A	VBATT
B	MODE
C	VMAIN
D	GND

* The pin designations in the table and illustration above (A, B, C, and D) are for illustration purposes only; these do not appear on the connector or the power supply.

Display

Table 1-31 gives the specifications of the LCD and Table 1-32 gives the pin assignments for the LCD connector.

Table 1-31. Display Specifications

Function	Description
Type	10-inch diagonal (9.5-inch active area), black and white FSTN liquid-crystal display non-glare surface VGA-compatible (640 × 480); 10:1 contrast ratio; CCFT sidelit; 32-shade gray scale
Writing surface	1.1 mm coated glass above LCD surface
Power	5 VDC, 12 VDC, 32 VDC, 800 – 1200 VAC @ 30 KHz

Table 1-32. LCD Display Connector Pin Assignments

Pin	Signal	Pin	Signal
1	VCONTRAST	11	UD0
2	VEE	12	UD1
3	GND	13	UD2
4	VDD	14	UD3
5	VLCD ON	15	LD0
6	Unused	16	LD1
7	LCDXSCLK	17	LD2
8	LCDLP	18	LD3
9	LCDFR	19	Unused
10	LCDFP	20	Unused

Digitizer

Table 1-32 gives the specifications of the digitizer and Table 1-33 gives the pin assignments for the digitizer connector.

Table 1-33. Digitizer Specifications

Function	Description
Type	Custom PCBA
Mounting	Below LCD

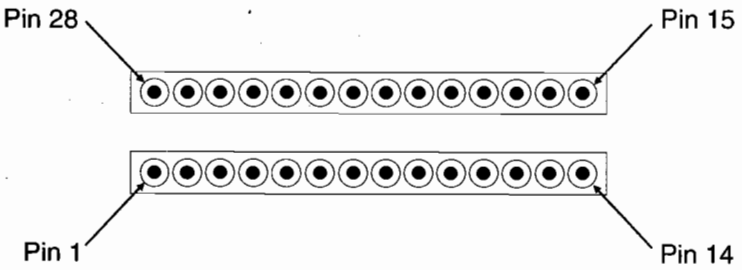


Figure 1-35. Digitizer Control Board Connector

Table 1-34. Digitizer Control Board Connector Pin Assignments

Pin	Signal	Pin	Signal
1	– 5V	15	WD7
2	– 5V	16	WD6
3	Unused	17	WD5
4	Unused	18	WD4
5	GND	19	WD3
6	GND	20	WD2
7	GND	21	WD1
8	+ 5V	22	WD0
9	+ 5V	23	BIRQ10
10	REFRESH#	24	PWRRESET#
11	BDIGICS#	25	Unused
12	IOR#	26	Unused
13	IOW#	27	Unused
14	SA1	28	Unused

Active low logic

Environmental Specifications

Table 1-35. Environmental Specifications

Environmental Condition	Operating	Non-Operating	Transportation
Temperature	0° C to 40° C	– 20° C to 60° C	n/a
Humidity (non-condensing)	10% to 80%	10% to 80%	n/a
Temperature cycling	48 hours, cycling 4 hours maximum and minimum, temperature 1° C/minute 10 cycles, 2 hours maximum	2 hours minimum, temperature 2° C/ minute	n/a
Vibration	0.5 G, 5 - 100 Hz 3 axes, 1 hour	1 G, 5 - 100 Hz 3 axes, 1 hour	2 G, 10 - 200 Hz 3 axes, random
Shock	5 G	50 G	n/a
Altitude (HDD)	10,000 ft. ASL	40,000 ft. ASL	40,000 ft. ASL

Regulatory and Safety Agency Information

CISPR	PUB.22 Class B
CSA	
FCC	PART 15, CLASS B
IEC 950	
TUV	
UL	
VDE	871 Class B self-certification

2. Removal and Replacement Procedures

2 Removal and Replacement Procedures

Contents

Figures

Introduction

Procedures for removing and replacing all of the pen computer's field-replaceable and/or field-repairable components and subsystems are provided in this chapter. To avoid repeating instructions that exist in earlier procedures, some procedures are referenced from within others. For example, in all procedures for removing internal components, the procedure for removing the case is referenced as the first step to avoid repeating the case-removal instructions.

All of the procedures are organized in sets of two, with the replacement procedure for a component or subsystem immediately following the removal procedure. Procedures for removing components or subsystems that are not serviceable in the field are not provided. For example, there is a procedure for removing the pen-digitizer/LCD-display subassembly, but there is no procedure for separating the LCD display from the digitizer, since these components are available as a complete subassembly only.

CAUTION

Some components of the pen computer are subject to damage from electrostatic discharge. Always use static-dissipating equipment, such as anti-static mats and wrist straps, when disassembling the computer and handling components, cables, and other subassemblies.

Case Removal

CAUTION

If the work surface where you will disassemble the computer has a hard surface that could scratch the computer's case, cover it with something that will cushion the computer, such as an anti-static rubber mat or a piece of anti-static packaging.

1. Remove the battery-compartment door, remove the battery pack, and remove the pen from its storage slot.
2. Place the computer on your work surface with the screen facing down and the I/O-connector covers facing you.
3. Remove the three screws at the I/O-connector end of the computer. These screws hold the front and back halves of the case together (see Figure 2-1).
4. Open all three I/O-connector covers.
5. Place the computer in your lap with the screen facing you and the I/O-connector end facing up.
6. Using only your fingers, gently pry the two halves of the case apart approximately 1/8-inch at the I/O-connector end, and carefully remove the three I/O-connector covers.
7. Keeping the computer in your lap, turn it around so the screen is facing away from you and the I/O-connector end is facing up.
8. Using both thumbs, carefully pry the center portion of the front half of the case (the half that frames the screen) up until you feel it snap past the catch on the edge of the chassis (see Figure 2-2).
9. Place the computer back on your work surface with the screen facing up.
10. Lift the front of the case at the I/O-connector end until it is perpendicular to the chassis, lift it off, and place it aside (see Figure 2-3).

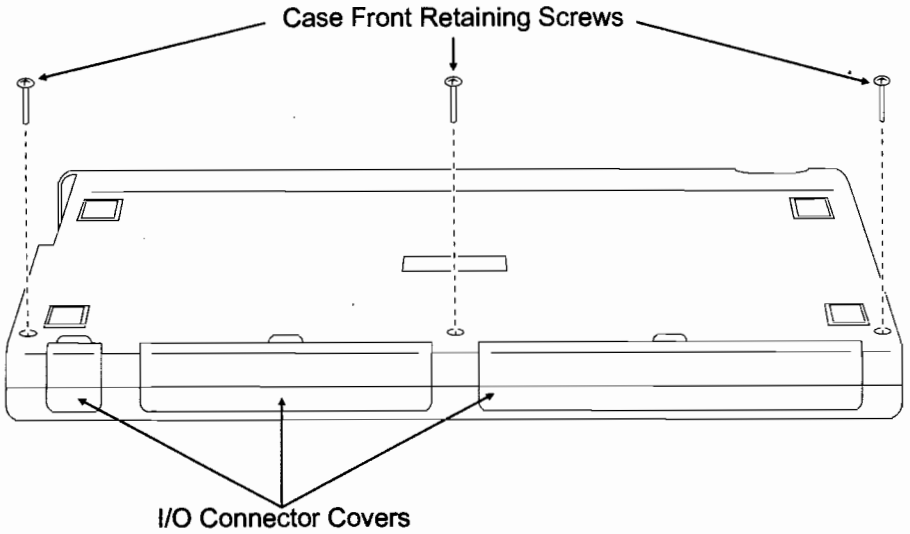


Figure 2-1. The Case Front Retaining Screws

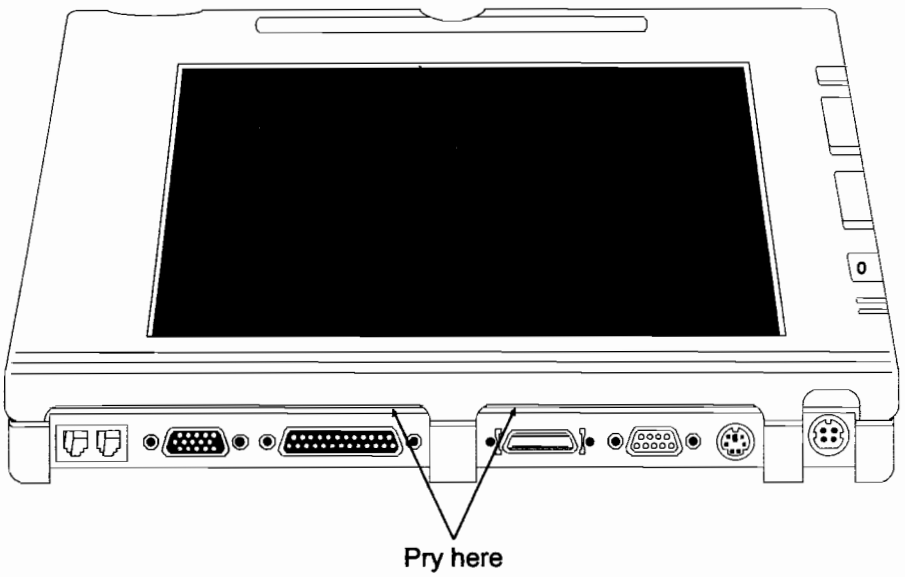


Figure 2-2. Releasing the Case Front

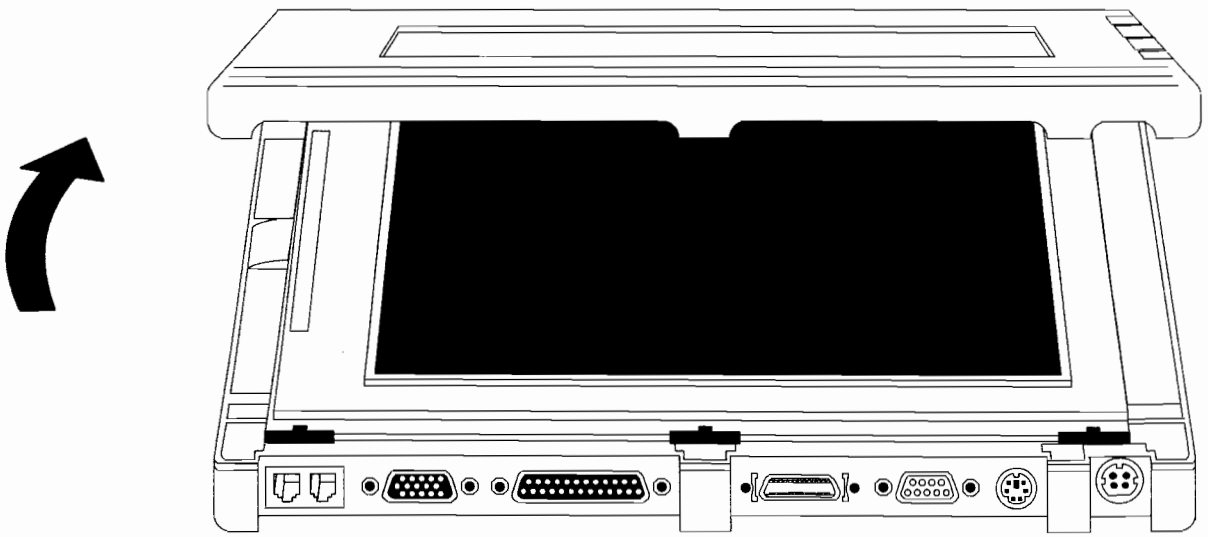


Figure 2-3. Removing the Case Front

11. Place the computer on your work surface with the screen facing down and the I/O connectors facing your body.
12. Remove the screw that attaches the back half of the case to the computer chassis (see Figure 2-4).

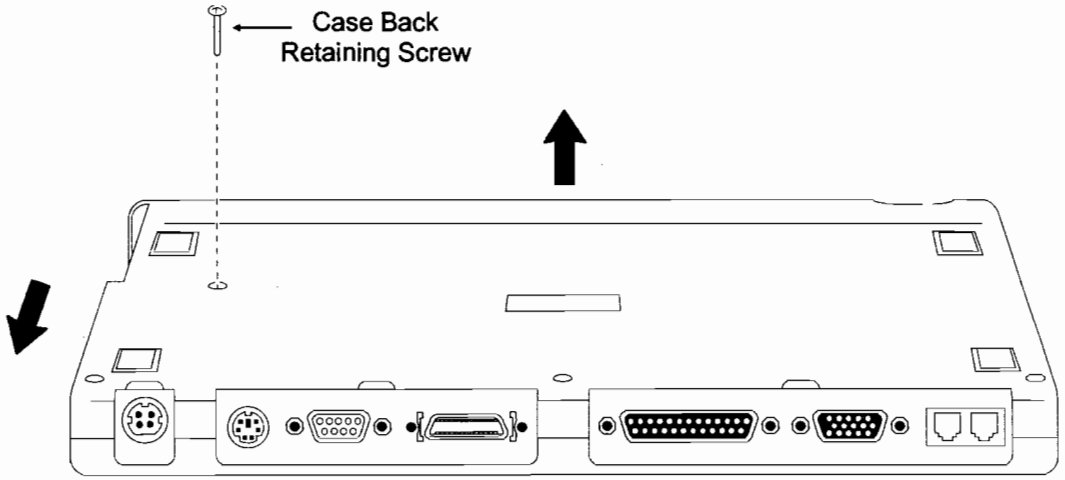


Figure 2-4. Removing and Replacing the Case Back

13. Lift the far end of the case back (the end opposite the I/O connectors) up slightly, and slide the case back towards you until the I/O connectors are free of their openings.
14. Lift the back of the case off the chassis, and place it aside.

Case Replacement

1. Place the computer chassis on your work surface with the screen facing down and the I/O-connector end facing your body.
2. Position the back half of the case over the chassis so that the I/O connectors pass through the connector openings in the case back, and lower it fully onto the chassis.
3. Insert the screw that attaches the case back to the chassis (see Figure 2-4).
4. Turn the computer over so the screen is facing up.
5. Slide the contrast and brightness controls all the way toward the DC/AC inverter, and check the power switch to be sure it is off (switch actuator towards the DC/AC inverter).
6. Position the case front so it is perpendicular to the chassis, and place it against the case back so the five sets of tabs on the edge of the case front are in the slots in the edge of the case back (the tabs and slots are on the edges opposite the connector openings).
7. Slide the power, contrast, and brightness buttons all the way toward the pen storage slot.
8. Pivot the case front down until it touches the chassis, and press down on the center of the I/O-connector edge of the case front until it latches.
9. Spread the case halves slightly, and insert the three connector covers in their slots.
10. Replace the three screws at the I/O-connector end of the computer (see Figure 2-1).
11. Inspect the joint where the two halves of the case fit together on all four sides of the computer to be sure the case is properly reassembled. Press the halves of the case together to latch them fully and to eliminate any gaps that remain.

Hard Disk Drive Removal

1. Remove the case (see page 2-3).
2. Place the computer on your work surface with the screen facing down and the I/O connectors facing your body.
3. Disconnect the HDD (hard disk drive) cable from the connector on the system board (CN5) by gently lifting the end of the cable while pressing down on the system board (see Figure 2-5).

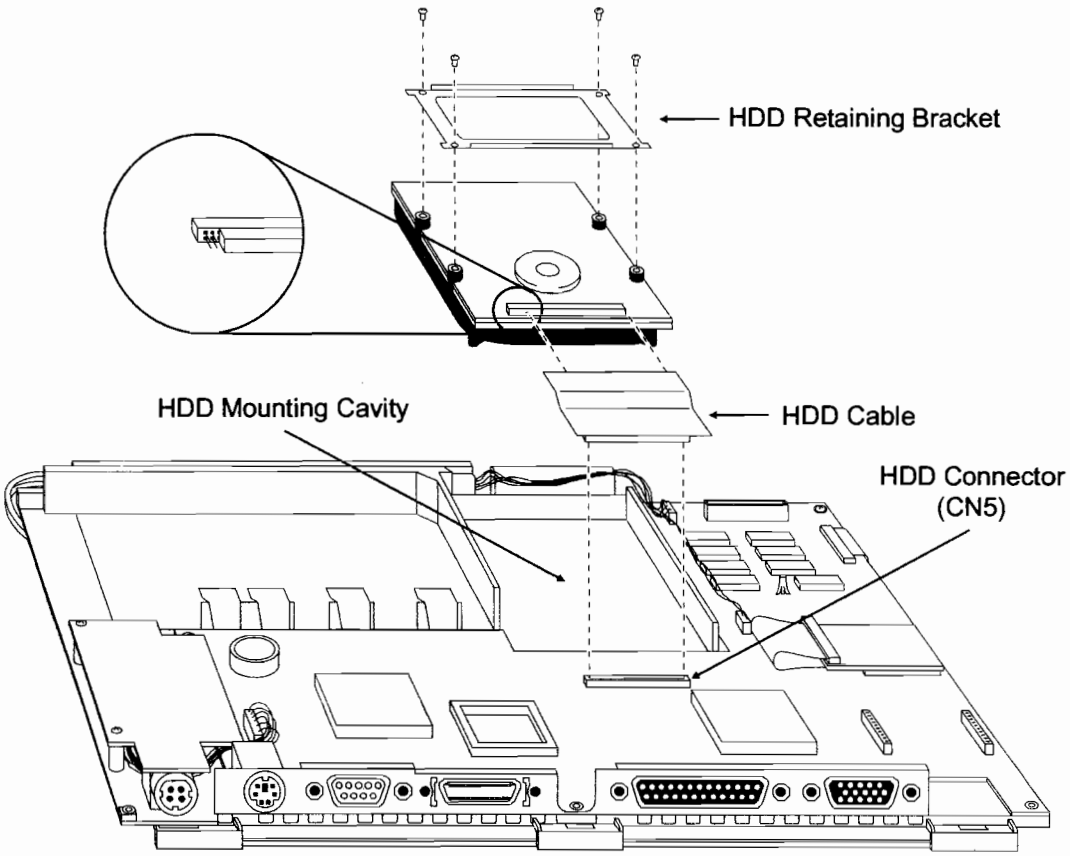


Figure 2-5. Removing and Replacing the Hard Disk Drive

4. Grasp the HDD retaining bracket by the raised edges with one hand while gently pressing either side of the plastic HDD mounting cavity away from the drive with the other hand.
5. When the retainer on the side wall of the drive cavity is clear of the retaining bracket, lift the drive out of the cavity, and place it on your work surface.

NOTE

If you do not intend to replace or service the existing hard disk drive, do not perform steps six through eight.

6. Remove the four screws that attach the HDD retaining bracket to the drive.
7. Lift the retaining bracket off the drive and place it aside.
8. Disconnect the hard HDD from the drive by pulling it away from the connector end of the drive.

Hard Disk Drive Replacement

1. Place the hard disk drive on you work surface with the circuit board facing up.
2. Place the HDD retaining bracket on top of the drive so the raised edges are pointing up and the holes in the bracket are aligned with the threaded holes in the drive frame (see Figure 2-5).
3. Insert a screw in each of the four holes in the drive bracket, and tighten the screws.
4. Position the HDD cable so the horizontal connector is aligned with the connector on the hard disk drive and the vertical connector is pointing down. Note that the connector on the cable is narrower than the one on the drive. When these connectors are properly aligned, the four pins at the left end of the drive connector (as shown in Figure 2-5) are exposed.
5. Connect the HDD cable to the drive.
6. Place the computer chassis (with the case removed) on your work surface with the screen facing down and the I/O connectors facing your body.
7. Position the drive over the mounting cavity with the connector end facing the I/O-connector end of the system board.
8. Lower the drive into the drive cavity.
9. Inspect the retaining tabs on the drive cavity side walls to be sure they have snapped over the ends of the retaining bracket. If they haven't, be sure the drive is properly aligned and all the way down in the mounting cavity.
10. Align the connector on the free end of the HDD cable with the connector on the system board (CN5), and press down on the end of the cable above the connector until it is fully inserted.
11. Replace the case (see page 2-5).

DC/DC Power Supply Removal

1. Remove the case (see page 2-3).
2. Place the computer on your work surface with the screen facing down and the I/O connectors facing your body.
3. Remove the two power-supply retaining screws (see Figure 2-6).

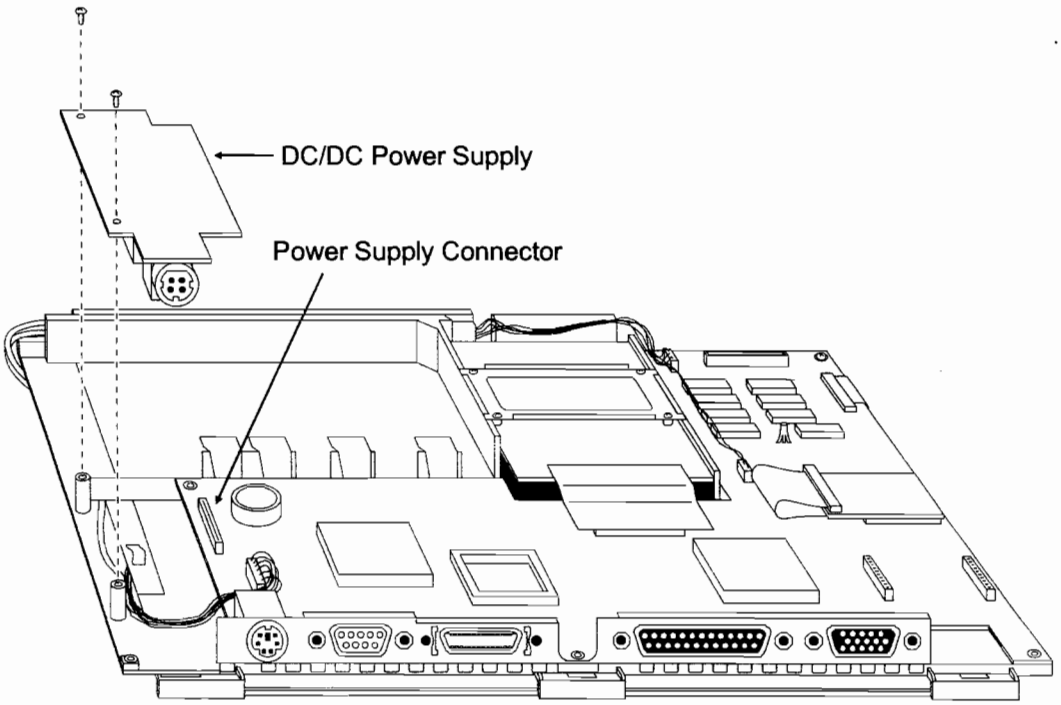


Figure 2-6. Removing and Replacing the DC/DC Power Supply

4. Lift the power supply straight up to disconnect it and remove it from the computer.

DC/DC Power Supply Replacement

1. Place the computer (with the case removed) on you work surface with the screen facing down and the I/O connectors facing your body.
2. Position the DC/DC power supply over the computer so the power-input connector is facing you and the circuit board is facing up (see Figure 2-6).
3. Align the two mounting holes in the left side of the power-supply circuit board with the two threaded mounting posts on the computer chassis. Make sure the power-supply connector on the underside of the power supply is aligned with the power-supply connector on the system board (SJ2), and press down until the connectors are fully mated.
4. Insert a screw in each of the two power-supply mounting holes and tighten the screws.
5. Replace the case (see page 2-5).

DC/AC Inverter Removal

1. Remove the case (see page 2-3).
2. Place the computer on your work surface with the screen facing down.
3. Disconnect the CCFT connector at the left end of the inverter (as shown in Figure 2-7).

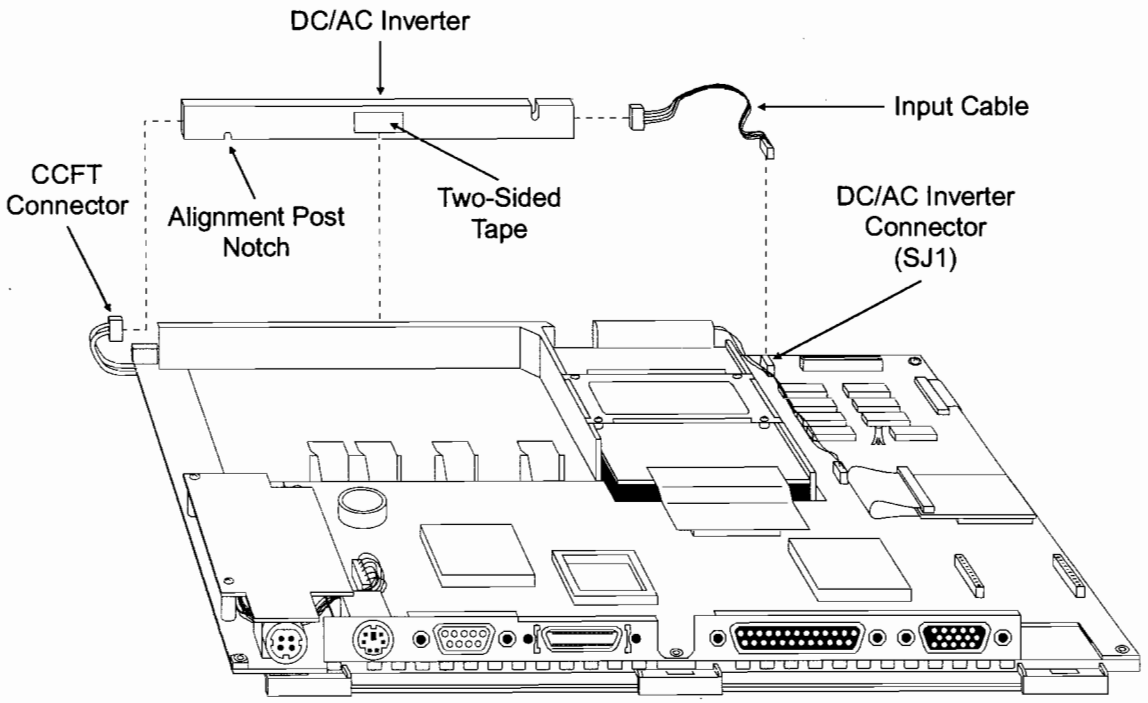


Figure 2-7. Removing and Replacing the DC/AC Inverter

4. Disconnect the inverter input cable from connector SJ1 on the system board.
5. Carefully pull the inverter assembly away from the chassis to detach the two-sided tape that attaches it.

CAUTION

Do not twist or turn the inverter when removing it. Keep the inverter parallel to the chassis until the tape is completely detached to avoid breaking the alignment post on the side of the chassis. Figure - shows the notch in the inverter that the alignment post fits into.

6. Remove any residual adhesive from the two-sided tape from the outside surface of the chassis.
7. Disconnect the input cable from the inverter by pulling it straight out of the end of the assembly.

DC/AC Inverter Replacement

1. Insert either end of the DC/AC inverter input cable into the connector on the right end of the inverter, as shown in Figure 2-7.
2. Remove the paper covering from the two-sided tape on the inverter.
3. Place the computer on your work surface with the screen facing down.
4. Make sure there is no residual adhesive left on the chassis from the tape on the old inverter.
5. Position the inverter as shown in Figure 2-7, orient it so the alignment post on the chassis fits into the notch at the bottom edge of the inverter shielding, and press the inverter firmly against the side of the chassis.
6. Insert the connector on the free end of the inverter input cable into connector SJ1 on the system board.
7. Insert the 2-pin connector on the CCFT cable into the connector at the left end of the inverter .
8. Replace the case (see page 2-5).

Bridge Battery Removal

1. Remove the case (see page 2-3).
2. Place the computer on your work surface with the screen facing down.
3. Disconnect the bridge-battery cable from connector BA1 on the system board (see Figure 2-8).

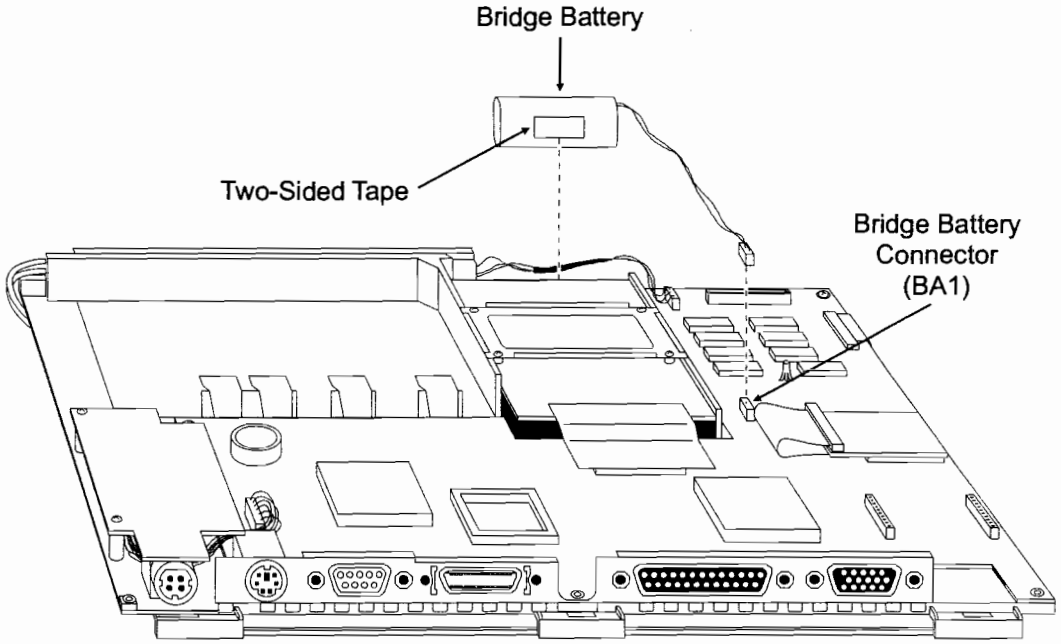


Figure 2-8. Removing and Replacing the Bridge Battery

4. Carefully pull the bridge battery away from the chassis to detach the double-sided tape that attaches it.
5. Remove any residual adhesive from the tape that attached the battery to the chassis.

Bridge Battery Replacement

1. Remove the paper covering from the two-sided tape on the new bridge battery.
2. Place the computer on your work surface with the screen facing down.
3. Make sure there is no residual adhesive left on the chassis from the tape on the old bridge battery.
4. Position the bridge battery as shown in Figure 2-8, align it with the DC/AC inverter (the battery should be centered vertically on the side of the chassis to avoid interference with the case when reassembling the computer), and press it firmly against the side of the chassis.
5. Insert the 2-pin connector on the end of the bridge battery cable into connector BA1 on the system board.
6. Replace the case (see page 2-5).

System Board Removal

1. Remove the case (see page 2-3).
2. Remove the DC/DC power supply (see page 2-8).
3. Remove the hard disk drive (see page 2-6).
4. If the optional fax/data modem is installed, remove it by pulling it straight up from the system board. Wrap the modem in anti-static packaging material, and place it aside (for additional information, see page 3-4).
5. If either of the optional memory-expansion boards is installed, remove the board by pulling it straight up from the system board. Wrap the memory board in anti-static packaging material, and place it aside (for additional information, see page 3-5).
6. Disconnect the following cables from the system board (see Figure 2-9):

   DC/AC inverter input cable (SJ1)
   LCD display cable (CN1)
   Digitizer cable/control board (JP2)
   Bridge battery cable (BA1)
   Control PCBA cable (CN8)

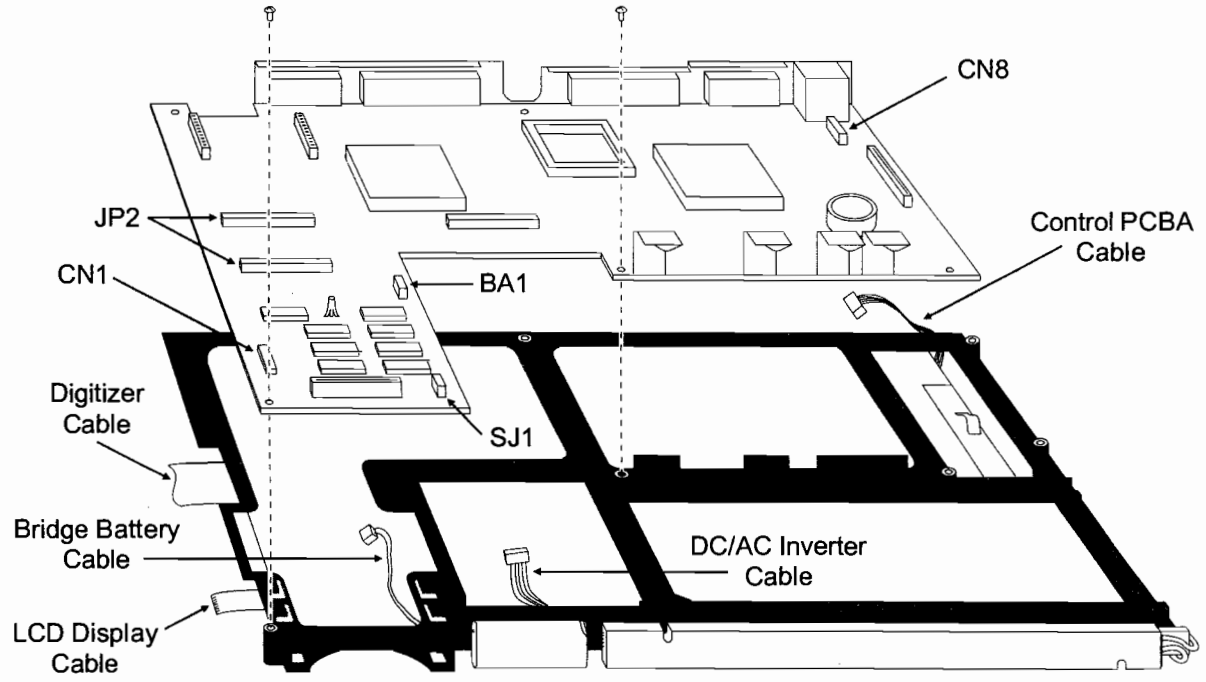


Figure 2-9. Removing and Replacing the System Board

7. Remove the two screws that attach the system board to the chassis.
8. Lift the system board off the chassis.

CAUTION

If you won't be working with the system board immediately, place it in anti-static packaging to prevent damage from static discharge.

System Board Replacement

1. Place the computer chassis on your work surface with the screen facing down and the DC/AC inverter facing your body, as shown in Figure 2-9.
2. Position the system board over the chassis with the battery-contact side facing up and the I/O connectors facing away from you.
3. Lower the system board into position so that the mounting holes in the board line up with the threaded mounting posts on the chassis. Be careful not to trap any of the cables from the control PCBA, the DC/AC inverter, the bridge battery, the LCD display, or the digitizer between the system board and the chassis.
4. Align the system board so the threaded holes in the mounting posts are visible through the mounting holes in the board.
5. Insert a screw in each of the two mounting holes shown in Figure 2-9, and tighten the screws.
6. Insert the connectors on the following cables in their corresponding connectors on the system board:

   DC/AC inverter input cable (SJ1)
   LCD display cable (CN1)
   Digitizer cable/control board (JP2)
   Bridge battery cable (BA1)
   Control PCBA cable (CN8)

7. If either of the optional memory-expansion boards was previously installed, replace the board (see page 3-4).
8. If the optional fax/data modem was installed, replace it (see see page 3-5).
9. Replace the hard disk drive (see page 2-7).
10. Replace the DC/DC power supply (see page 2-8).
11. Replace the case (see page 2-5).

Control PCBA Removal

CAUTION

While it is possible to remove the control PCBA without removing the DC/DC power supply and disconnecting the control PCBA cable from the system board, this is not recommended. Since there is very little slack in the control PCBA cable, it is difficult to disconnect it from the control PCBA without damaging the cable, the control PCBA, or one of the connectors.

1. Remove the case (see page 2-3).
2. Remove the DC/DC power supply (see page 2-8).
3. Place the computer chassis on your work surface with the screen facing down and the I/O connectors facing your body.
4. Disconnect the control PCBA cable from connector CN8 on the system board (see Figure 2-10).

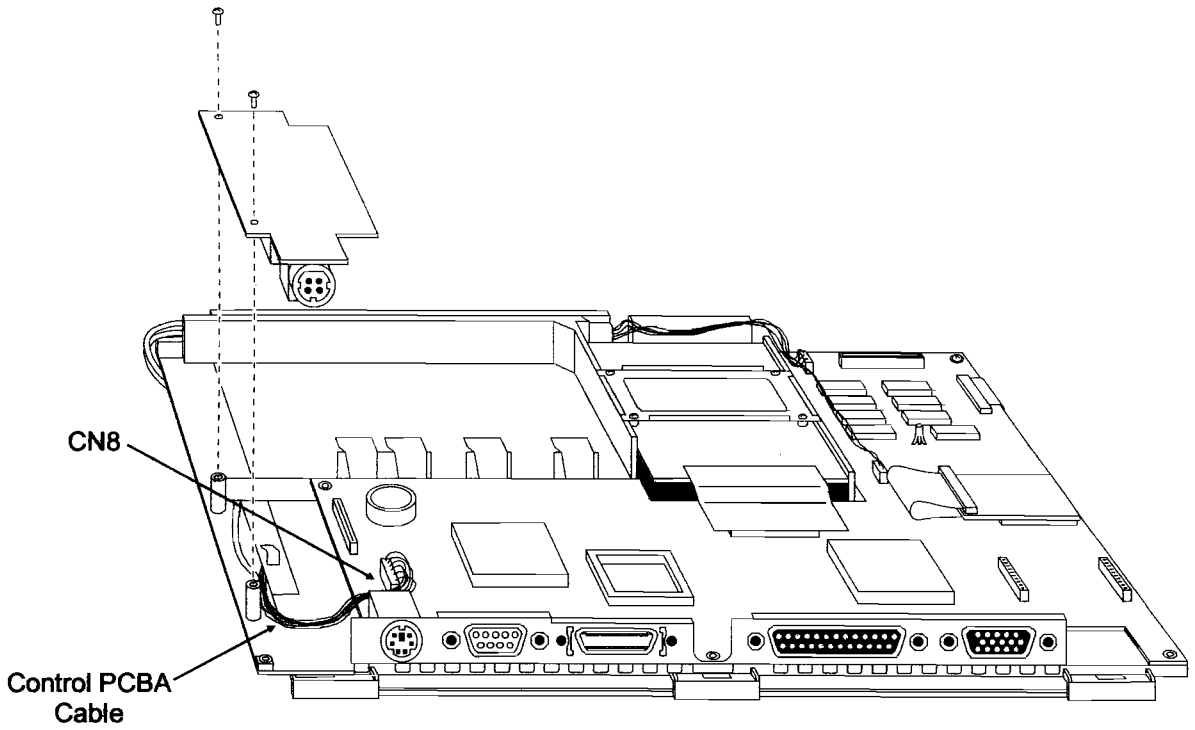


Figure 2-10. Connecting or Disconnecting the Control PCBA Cable

5. Turn the computer over so the screen is facing up and the control PCBA is on your right, as shown in Figure 2-11.
6. Remove control PCBA retaining screw (at the end of the control PCBA closest to you).
7. Lift the near end of the control PCBA up approximately ½-inch, and pull the board toward you approximately ½-inch to disengage the slot in the far end of the board from the mounting clip on the chassis.
8. Guide the cable through its opening as you lift the control PCBA clear of chassis.
9. Carefully disconnect the cable from the control PCBA by pulling it away from the board, as shown in Figure 2-11.

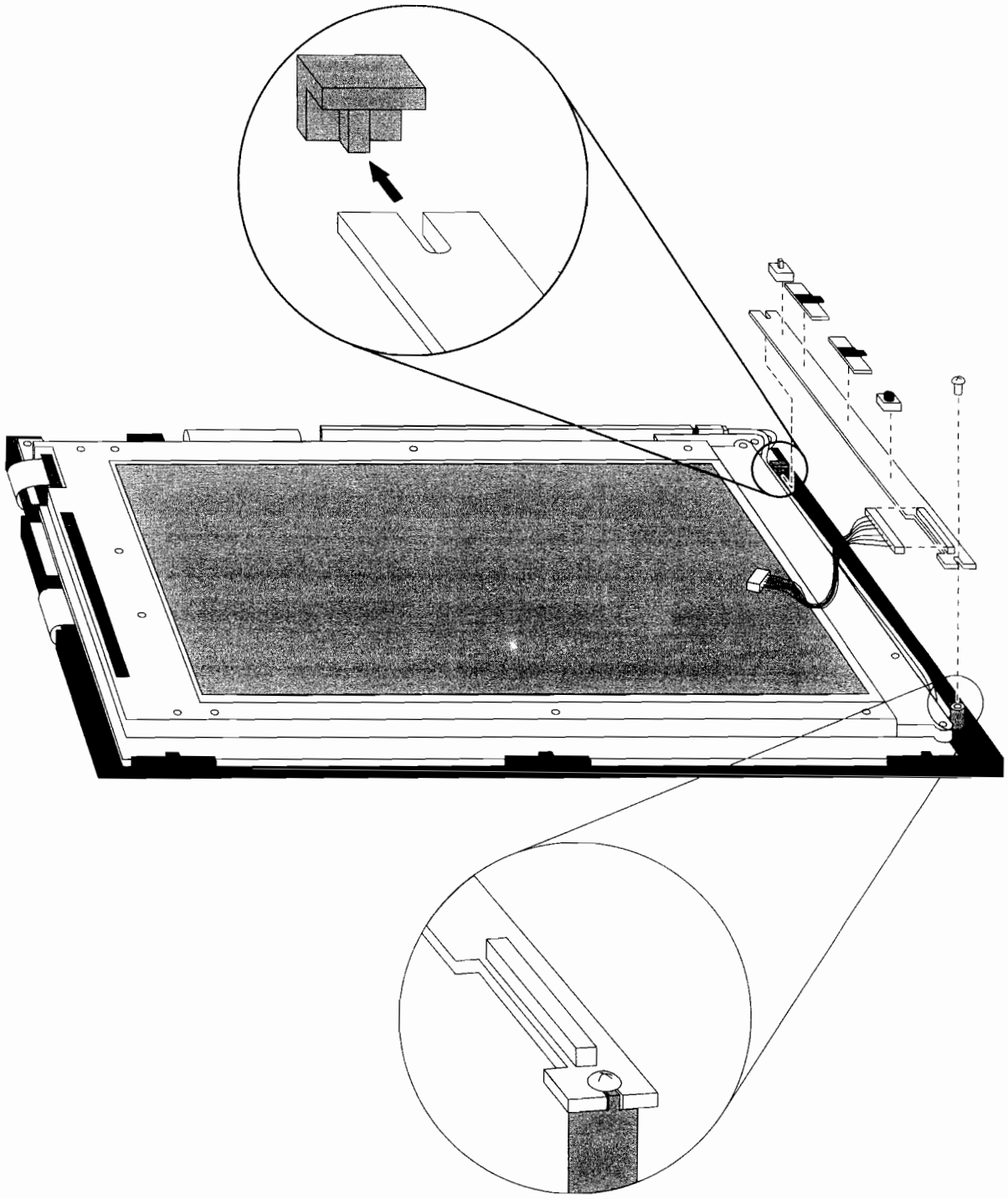


Figure 2-11. Removing and Replacing the Control PCBA

NOTE

The power switch, the contrast and brightness potentiometers, and the Suspend/Resume switch can be replaced separately. Use standard soldering techniques to remove and replace these components.

Control PCBA Replacement

1. Place the computer chassis on your work surface with the screen facing up and the LCD and digitizer ribbon cables at the left side.
2. Connect the control PCBA cable to the control PCBA as shown in Figure 2-11.
3. Insert the free end of the control PCBA cable through the opening in the chassis at the edge of the LCD-display frame. The long lead from the display backlight (CCFT) should be between the control PCBA cable and the display frame.
4. Insert the far end of the control PCBA (the power-switch end) under the retaining tab on the chassis so that the notch in end of the board fits around the vertical locating post (see Figure 2-11).
5. Lower the near end of the control PCBA (guide the cable through the opening in the chassis) until the board is resting on the front mounting post. The rectangular extension at the top of the mounting post should fit into the end of the notch in the board.
6. Insert the retaining screw through the gap between the mounting post extension and the inner end of the notch, and tighten the screw.
7. Turn the computer over so the screen is facing down and the I/O connectors are facing your body.
8. Connect the free end of the control PCBA cable to CN8 on the system board (see Figure 2-10).
9. Replace the DC/DC power supply (see page 2-8).
10. Replace the case (see page 2-5).

Screen/Digitizer Subassembly Removal

1. Remove the case (see page 2-3).
2. Place the computer on your work surface with the screen facing down and the I/O connectors facing away from your body.

NOTE

If the optional fax/data modem and/or one of the optional memory-expansion boards is installed, remove these options from the computer before performing steps 3 and 4 to provide additional working space.

3. Disconnect the LCD display cable from connector CN1 on the system board (see Figure 2-12).

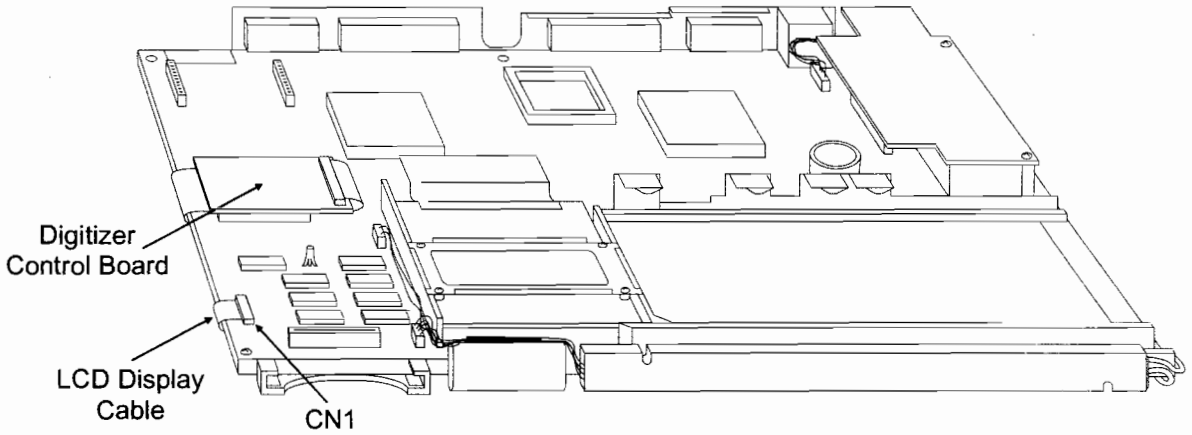


Figure 2-12. Connecting or Disconnecting the LCD Cable and the Digitizer Control Board

4. Disconnect the digitizer control board from connector JP2 by carefully pulling it straight up from the system board. Work carefully to avoid bending any of the pins on the control board or overstressing the attached ribbon cable.
5. Disconnect the ribbon cable from the connector on the digitizer control board, and place the control board aside.
6. Remove the screw that attaches the screen/digitizer subassembly to the chassis, as shown in Figure 2-13.
7. Lift the near end of the chassis approximately ½-inch, and slide the chassis away from you until it disengages from the clips at the far edge. Place the chassis (with the system board and other components attached) aside.

NOTES

The screen, the backlight, and the digitizer assembly are not field repairable, and the individual components of this subassembly are not replaceable separately.

To remove only the digitizer control board, perform steps 1, 2, 4, and 5 of the above procedure.

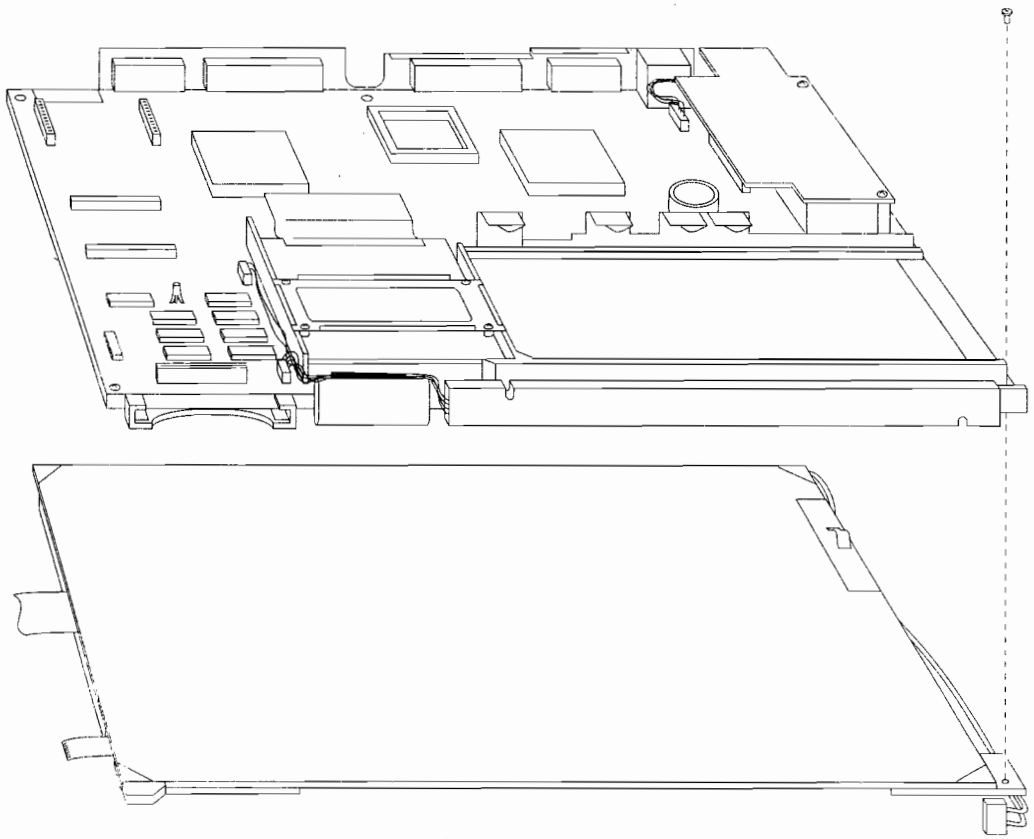


Figure 2-13. Removing and Replacing the Screen/Digitizer Subassembly

Screen/Digitizer Subassembly Replacement

1. Place the screen/digitizer subassembly on your work surface with the screen facing down and the ribbon cables at your left.
2. Position the chassis over the screen/digitizer subassembly with the system board facing up and the I/O connectors facing away from your body, as shown in Figure 2-13.
3. Tilt the far edge of the chassis down slightly, allow it to rest on the far edge of the screen/digitizer subassembly, and slide the chassis towards you so the clips on the far edge of the chassis engage the edge of the screen/digitizer subassembly.
4. Lower the near edge of the chassis until it is resting on the screen/digitizer subassembly.
5. Insert and tighten the retaining screw, (see Figure 2-13).
6. Connect the ribbon cable from the digitizer to the digitizer control board.
7. Turn the chassis over, and carefully position the digitizer control board over the two halves of connector JP2 on the system board. Check the positions of all the pins on the control board before pressing down on the board to connect it. Refer to Figure 2-12.

NOTE

The digitizer ribbon cable should pass under the control board (see Figure 2-12).

8. Connect the ribbon cable from the LCD display to connector CN1 on the system board.
9. If you removed a fax/data modem and/or a memory-expansion board for better access to the digitizer control board and the LCD cable, replace these items now.
10. Replace the case (see page 2-5).

3. Optional Equipment

3 Optional Equipment

Contents

Figures

Tables

Available Options

Table 3-1 lists the options available for the pen computer system. Procedures for installing all internal options follow the table.

CAUTION

Always use static-electricity protection, such as static-dissipating mats and wrist straps, when handling the computer's components and internal options.

Table 3-1. Optional Equipment

Item	Description
Fax/Data Modem	Combined 9600 bps send/receive fax and 2400 bps data internal modem
4 MB Memory Board	Plug-in memory board provides an additional 4 MB RAM for a total of 8 MB
16 MB Memory Board	Plug-in memory board provides an additional 16 MB RAM for a total of 20 MB
Numeric Coprocessor	Socket on system board accepts Intel 80387SX (or compatible) coprocessor
NOTE The following options do not require installation:	
External Battery Charger	The external charger allows the user to charge battery packs outside the computer. The charger is powered by the AC adapter that is provided with the computer or by the optional automotive power adapter.
Automotive Power Adapter	The automotive power adapter converts the 12 VDC, negative ground power available in most vehicles to 17 VDC for input to the computer or the external charger.
Diskette Drive	The external 3½-inch diskette drive connects to the computer through the FDD connector. This drive is compatible with the 720 KB and 1.44 MB formats used on IBM-compatible PC's.
Carrying Case	The leather carrying case includes a shoulder strap and has compartments for the computer, the AC adapter, diskettes, and optional equipment.
Other options	Additional battery packs, AC adapters, and pens are also available as options.

Modem Installation

1. Remove the case (see page 2-3)
2. Position the chassis on your work surface with the screen facing down and the I/O-connector end facing your body (see Figure 3-1).

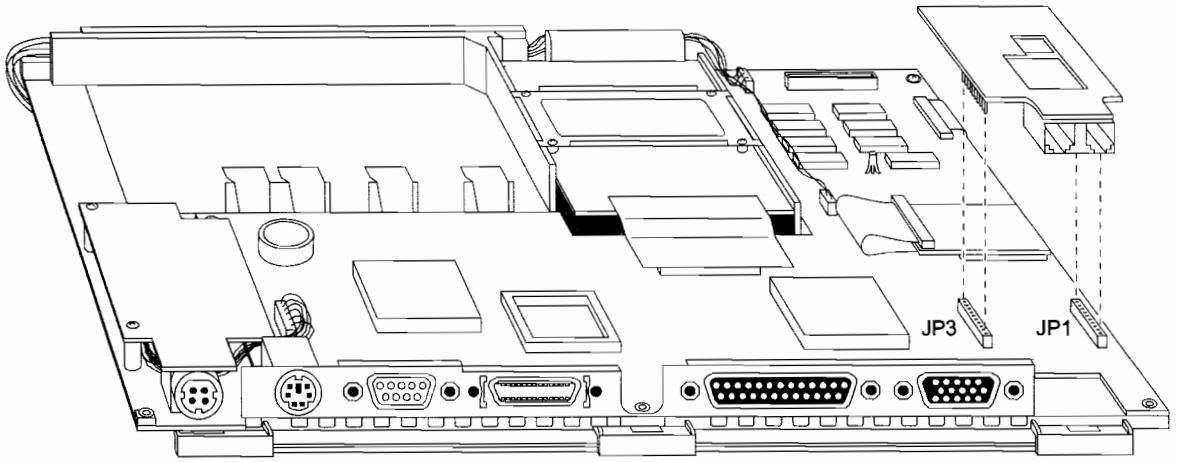


Figure 3-1. Installing and Removing the Internal Modem

3. Remove the internal modem from its packaging.
4. Position the internal modem over the system board so the two rows of male connector pins on the internal modem are aligned with the two female modem connectors (JP1 and JP3) on the system board. (The connector pins should be facing down, and the two RJ-11 telephone connectors should be facing you.)
5. Carefully align the pins on the internal modem connectors with the pin sockets in the modem connectors on the system board. Inspect each pin to be sure it is positioned correctly.
6. Press down gently on the internal modem until both connectors are fully inserted.
7. Press out the rectangular connector knockout in the bottom half of the case (at the end opposite the opening for the power-input connector). Use a file or a knife to trim off any plastic left behind from the knockout. Do not allow the plastic knockout or any of the plastic trimmed from the case to fall into the computer.
8. Replace the case (see page 2-5).
9. Check the modem for proper operation using a communications or diagnostic program that is capable of testing the modem's fax and data modes of operation.

Modem Removal

1. Remove the case (see page 2-3)
2. Position the chassis on your work surface with the screen facing down and the I/O-connector end facing your body (see Figure 3-1).
3. Disconnect the modem from connectors JP1 and JP3 by lifting it straight up from the system board. Be careful not to pull the modem at an angle to avoid damaging the connectors.
4. Replace the case (see page 2-5).

Memory Expansion Board Installation

NOTE

The installation procedure is the same for the 4 and 16 MB memory-expansion boards.

1. Remove the case (see page 2-3)
2. Position the chassis on your work surface with the screen facing down and the I/O-connector end facing away from your body (see Figure 3-2).

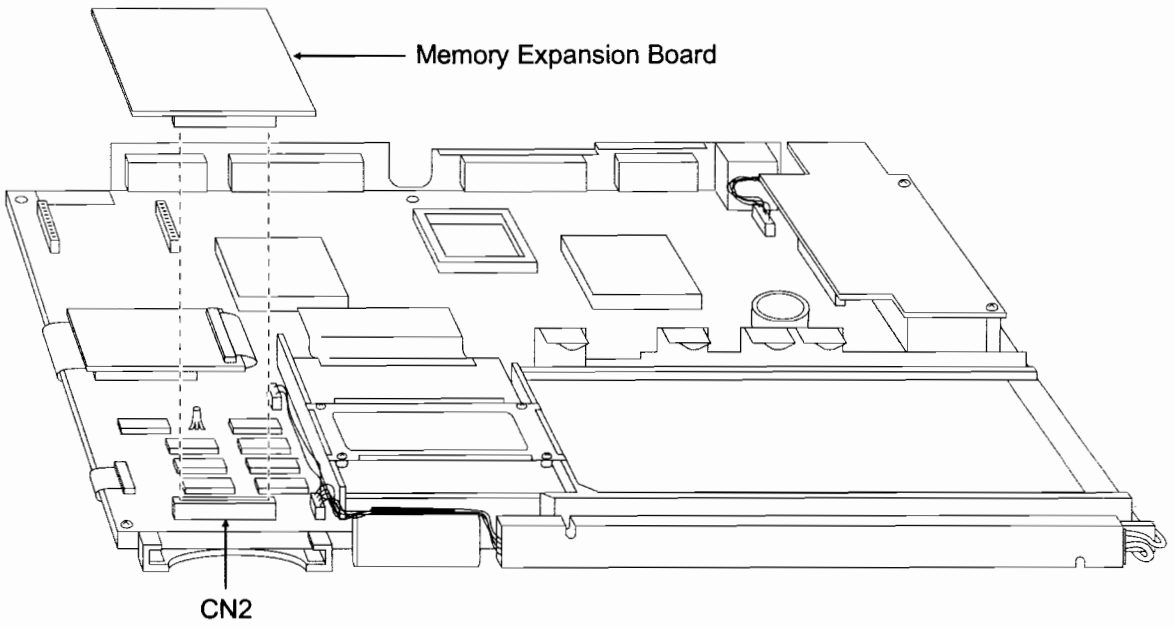


Figure 3-2. Installing and Removing the Memory Expansion Board

3. Remove the memory-expansion board from its packaging.
4. Position the memory-expansion board over the system board so the connector on the memory-expansion board is aligned with memory-expansion connector CN2 on the system board, as shown in Figure 3-2. (The connector should be facing down, and the connector end of the memory-expansion board should be closest to you.)
5. Insert the connector on the memory-expansion board into connector CN2 on the system board.
6. Press down gently on the memory-expansion board until the connector is fully inserted.
7. Replace the case (see page 2-5).
8. Turn on the computer, select the SETUP program, and verify that the amount of memory shown in the Total Sys Memory field is correct (8192 KB for a 4 MB memory-expansion board or 20480 KB for a 16 MB memory-expansion board).

Memory Expansion Board Removal

1. Remove the case (see page 2-3)
2. Position the chassis on your work surface with the screen facing down and the I/O-connector end facing away from your body (see Figure 3-2).
3. Disconnect the memory expansion board from connector CN2 by lifting it straight up from the system board.
4. Replace the case (see page 2-5).

Numeric Coprocessor Installation

1. Remove the case (see page 2-3)
2. Position the chassis on your work surface with the screen facing down and the I/O-connector end facing away from your body.

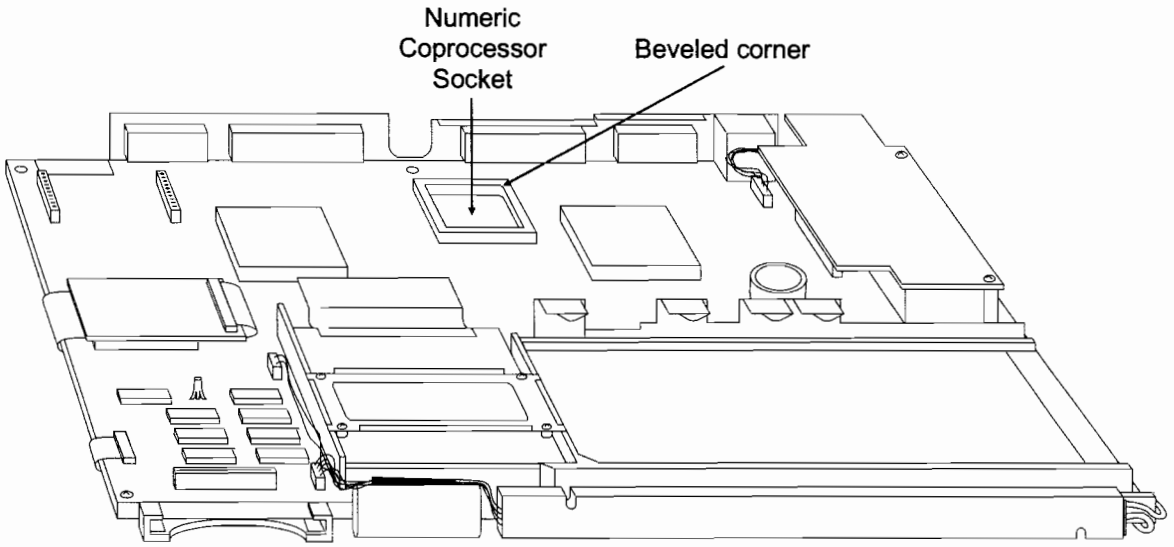


Figure 3-3. Installing and Removing the Numeric Coprocessor

3. Remove the numeric coprocessor chip from its packaging.
4. Position the coprocessor chip on the coprocessor socket so the beveled corner of the chip is aligned with the beveled corner of the socket (see Figure 3-3).
5. Press down on the chip until it is fully inserted in the socket. The top surface of the chip should be approximately even with the top surface of the socket.
6. Replace the case (see page 2-5).
7. Use a diagnostic program to test the numeric coprocessor for proper operation.

Numeric Coprocessor Removal

1. Remove the case (see page 2-3)
2. Position the chassis on your work surface with the screen facing down and the I/O-connector end facing away from your body.
3. Use a PLCC chip extractor to remove the coprocessor chip from the socket (see Figure 3-3).
4. Replace the case (see page 2-5).

4. Diagnostics

4 Diagnostics

Contents

Figures

What is the Diagnostic Program?

The diagnostic program is used to test the various components of the Pen Computer system. Since the program is modular, you can test each component individually. The diagnostic program also has an automatic test option, so you can test the hardware automatically and run the system overnight. The diagnostic program consists of the following files:

LOADER.COM	**DIAG.SUB**	**PENCAL.EXE**	**PENDIAG.EXE**
TPCMCIA.COM	**VGA.EXE**	**HELP.DAT**	**KEYIN.DAT**
ERROR.REC			

LOADER.COM is the program that loads and runs *DIAG.EXE*.

DIAG.SUB is the main program of the diagnostic software.

PENCAL.EXE is the program that tests the calibration of the pen digitizer.

PENDIAG.EXE is the program that tests the diagnostic commands of the digitizer.

TPCMCIA.COM is the program that tests the *PCMCIA* device.

VGA.EXE is the program that tests EGA/VGA.

HELP.DAT is the file that contains help information.

KEYIN.DAT is the file that contains the order of the tests in the automatic test.

ERROR.REC is the file in which the error messages that occur testing are stored. This file only works in a DOS 3.x or higher environment.

How To Load The Diagnostic Program

Preparation

The following items are required for certain tests:

Blank diskette	Needed when testing the FDD
External serial loopback connector	Needed to test the serial port. See *Loopback Connection Structure*, page 4-18.
External parallel loopback connector	Needed to test the parallel port. See *Loopback Connection Structure*, page 4-18
PCMCIA card	Needed to test the PCMCIA device
Parallel printer	Needed to test the printer
Mouse	Needed to test the mouse
80386SX/20 math coprocessor	Needed to test the coprocessor

Installation

You can run the diagnostic program from the diskette or from the hard disk. If you want to run it from the diskette, insert the diagnostic program diskette into the diskette drive and load the program. If you want to run it from the hard disk, create a directory for the diagnostic program, copy all files from the diagnostic program diskette to the directory, and load the program from the hard disk. When you run the diagnostic program from the diskette, make sure you make a backup copy of the diskette before running it.

Loading

1. Select the drive that has the diagnostic program, type **LOADER**, and press **Enter**. The following screen is displayed.

NOTES

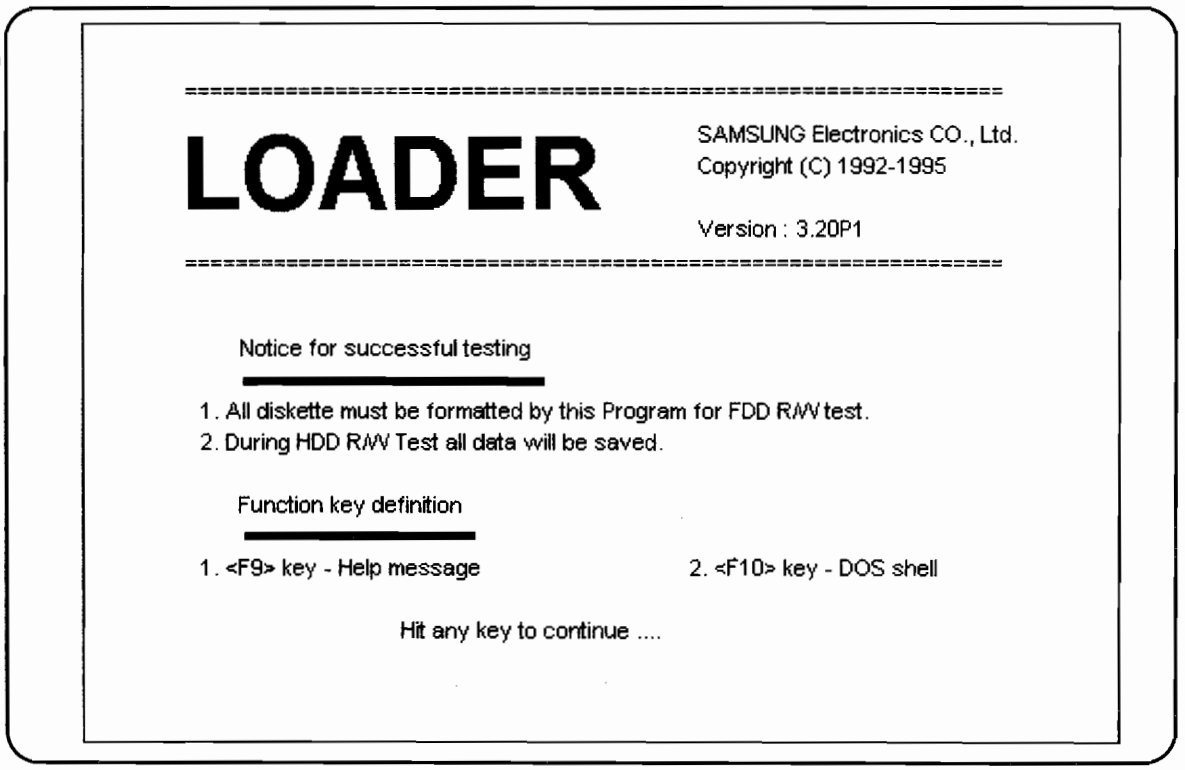


Figure 4-1. Initialization Screen

Diskettes used for diagnostic testing must be formatted with this program.

To view a help screen, press the **F9** key.

To shell to DOS, press the **F10** key. To return to the diagnostic program from the DOS prompt, type "exit," and press **Enter**.

2. Press **Enter** to proceed to the next step. You are now ready to run the diagnostic program.

Main Menu and Selections

Figure 4-2 shows the main menu of the diagnostic program.

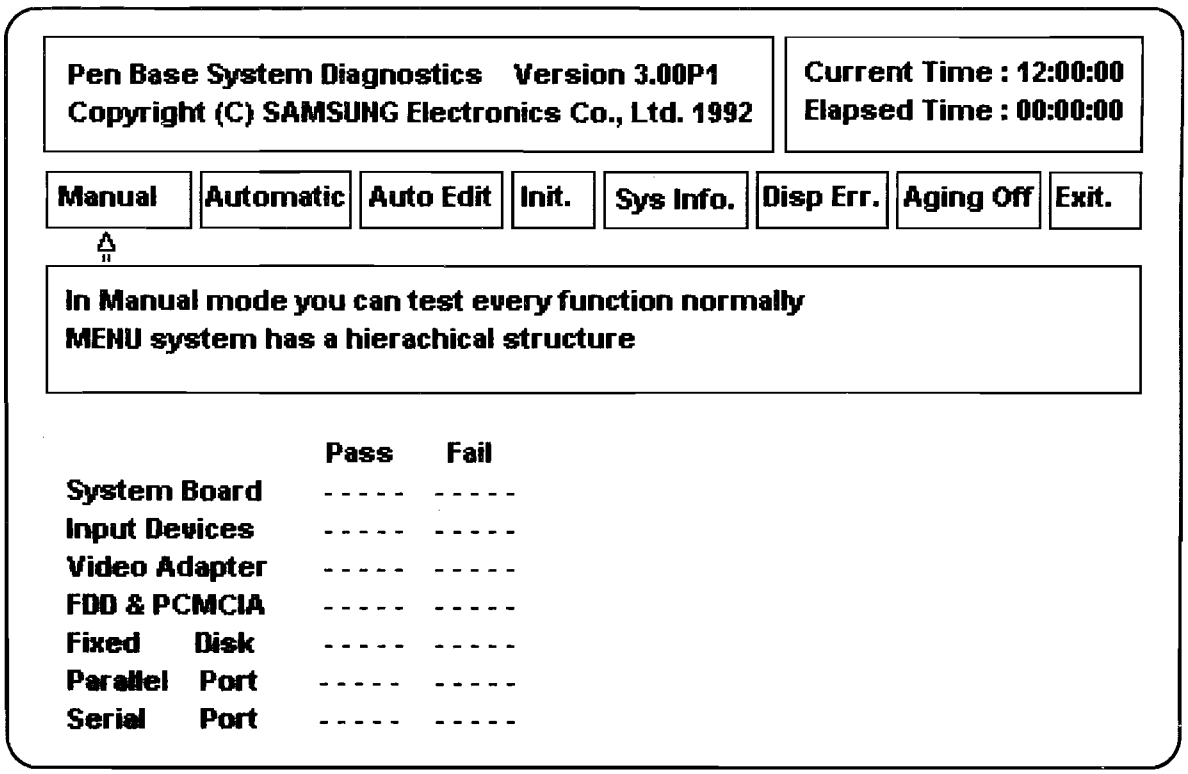


Figure 4-2. Main Menu

All menus have a vertical structure. The cursor is located initially under *Manual.* You move the cursor by using the the left or right arrow key. You invoke sub-menus by using the **Enter** or the down arrow key. You return to the previous menu by pressing **ESC** or the up arrow key. The *Quit* selection of the sub-menu has the same result.

Manual Test

Each component of the system can be tested manually. When a failure occurs, the appropriate error massage is displayed and you are asked if you want to save the error message. Type "Y" to save it, or type "N" or press **ESC** to discard it. If you type "Y", the error message is stored in the ERROR.REC file.

To select the manual test, position the cursor at *Manual* on the main menu and press **Enter**. Figure 4-3 shows the manual test menu.

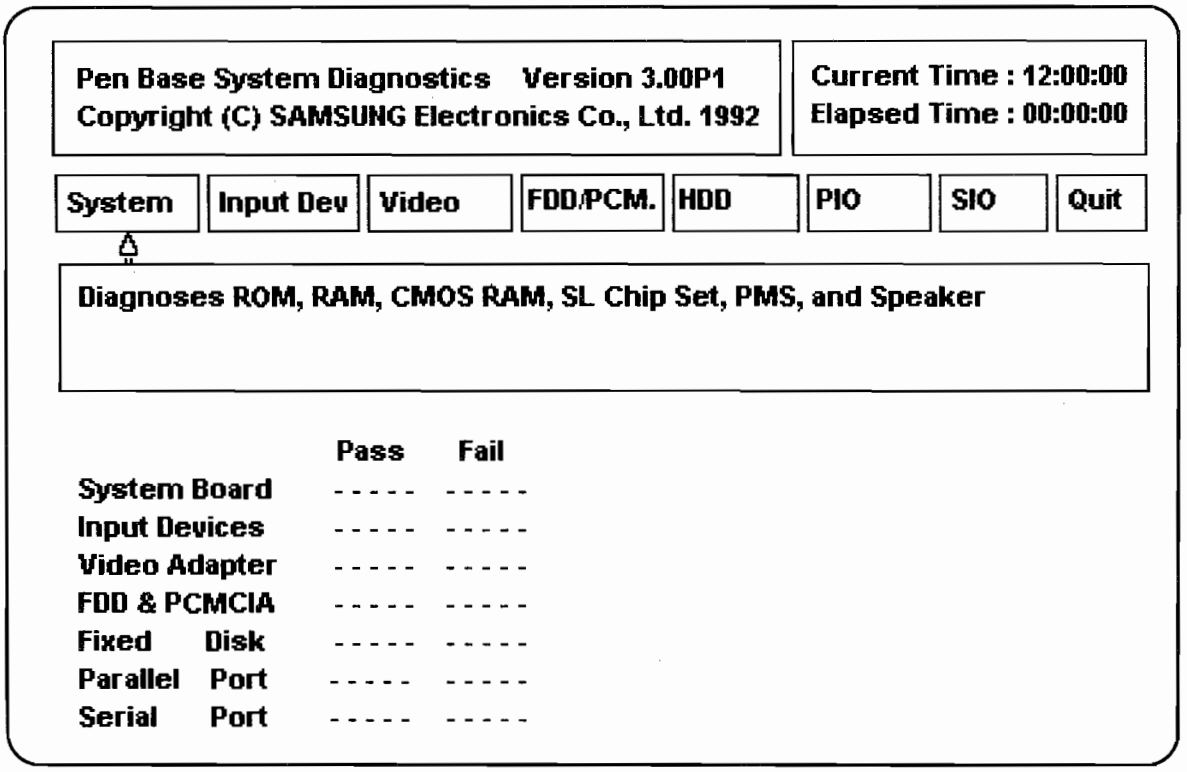


Figure 4-3. Manual Test Menu

The following sections describe the tests available for each manual test selection.

System

Coprocessor: Tests the data transfer and arithmetic functions of the coprocessor when installed.

ROM: Tests the checksums of the extended BIOS ROM and the system ROM modules.

RAM: Tests the 640 KB basic RAM and extended memory up to 4 GB. You can terminate the program during testing by pressing the **F8** key.

CMOS RAM: Tests the CMOS RAM. The current values of the CMOS RAM are saved and restored after testing is completed.

Speaker: Tests the speaker. You have to answer "Y" or "N" when the program asks you "`Did it sound good? (Y/N)`" after completing the test.

SL Chips: Tests the five main components of the 80386SL chipset: the Internal Bus Unit, the External Bus Unit, the Cache Unit, the On Board Memory Control Unit, and the 80386SL microprocessor and its registers.

PMS: Tests the local standby and the global standby of the power management. The PMS test is not affected by the SETUP.

Quit: Returns to the main menu. You can also return to the main menu by pressing **ESC** or the up arrow key.

Input Dev.

Reset KBD: Tests the reset command in the keyboard. Sends a reset command to the keyboard processor and receives the code value that indicates the reset is completed.

KBDC BAT: Tests the keyboard controller.

Scan Code: Tests all the possible keyboard scan codes. The keyboard is displayed on the screen and when you press a key, that key blinks on the screen. You have to make a decision if the keyboard is working correctly. When the test is finished, press the **ESC** key twice to exit from the test. The program supports several different keyboard la, outs. You can ignore all keyboard layouts except the US 101 and the UK 102 layouts.

Pen Test: Tests the diagnostic commands and the calibration of the pen digitizer. Before testing, you must adjust the pen using the SETUP utilities. The following tests are available:

Pen Diag.: Tests the diagnostic commands of the pen digitizer;
Calibrate: Tests the pen calibration of the pen digitizer;
Line Test: Asks the user to draw lines and verify that they are correct.

Mouse: Tests the movements of the mouse. The mouse device driver should be installed before testing.

Quit: Returns to the main menu.

Video

Mode Test: Tests the functions that can be displayed on the screen. If an EGA monitor is attached to the VGA card, only EGA display functions can be tested.

Chip Diag: Tests the EGA/VGA register, Video RAM, External Palette RAM, Read Mode 0/1, and Write Mode 0/1/2.

FDD

FDD Reset: Resets the diskette drive. If run in manual mode, it tests and displays the status of the diskette.

Format: Formats the diskette. You have to select the correct diskette type. After formatting, you can use the diskette as a DOS formatted diskette, but the external track 1, the middle track 2, and the internal track 1 will be checked as bad to establish the field that is needed while performing the FDD R/W test in this format. Thus, eight tracks of the FAT will be displayed as bad.

R/W Test: Tests the read/write functions of the drive, but does not test the quality of the diskette. If a bad sector is found, the sector will be marked and skipped in the next test.

Seeking: Tests random and sequential seek functions.

Motor Spd: Measures the speed of the diskette drive motor 10 times. The measured speed is displayed as maximum and minimum speeds in milliseconds.

PCMCIA: Tests the PCMCIA Device and formats the PCMCIA card if the card is inserted. You must install the PCMCIA Drive in CONFIG.SYS (IFS.SYS, FSLLD.SYS, FEFS.SYS, FLASH.COM).

Quit: Returns to the main menu.

HDD

HDD Reset: Tests the hard disk device controller.

Format: Performs an AT-standard hard disk low-level format. You can input the factory bad sector map and interleave.

R/W Test: Tests the read/write functions without destroying the current data. If the Aging mode is "On," all tracks are tested; only certain tracks are tested if theAging mode is "Off."

Seeking: Tests random and sequential seek functions of the hard disk drive head.

Scanning: Scans the surface of the hard disk and displays the error sector map.

Quit: Returns to the main menu.

PIO

Loopback: Tests the internal and external loopback and the interrupt line. You have to attach the loopback connector before running these tests.

Printer: Tests the printing functions. You have to attach the printer before running these tests.

SIO

You must attach the loopback connector before running these tests.

Manual: Select the port and internal or external mode. When the mode is internal, the data rate is 2400. When the mode is external, the data rate is 9600, 1200, and 150. All the combinations of parity, data bits, and stop bits are tested.

Auto: Tests all combinations of parity, data bits and stop bits with 9600/1200/150 data rates in both internal and external mode. Since COM2 does not have a physical port, the COM2 external loopback test will fail in this test.

Modem: Tests the internal modem.

A) **Setup**: Set the data rate of the modem. You must set the data rate before performing the mode tests.

B) **Ans. mode**: Tests the answer mode.

C) **Org. mode**: Tests the originate mode.

Quit

Quit: Returns to the main menu.

Automatic Test

The automatic tests are performed without any input from the user. The order of testing is defined in the KEYIN.DAT file.

To select the automatic tests, position the cursor at *Automatic* on the main menu and press **Enter**. Figure 4-4 shows the automatic test menu.

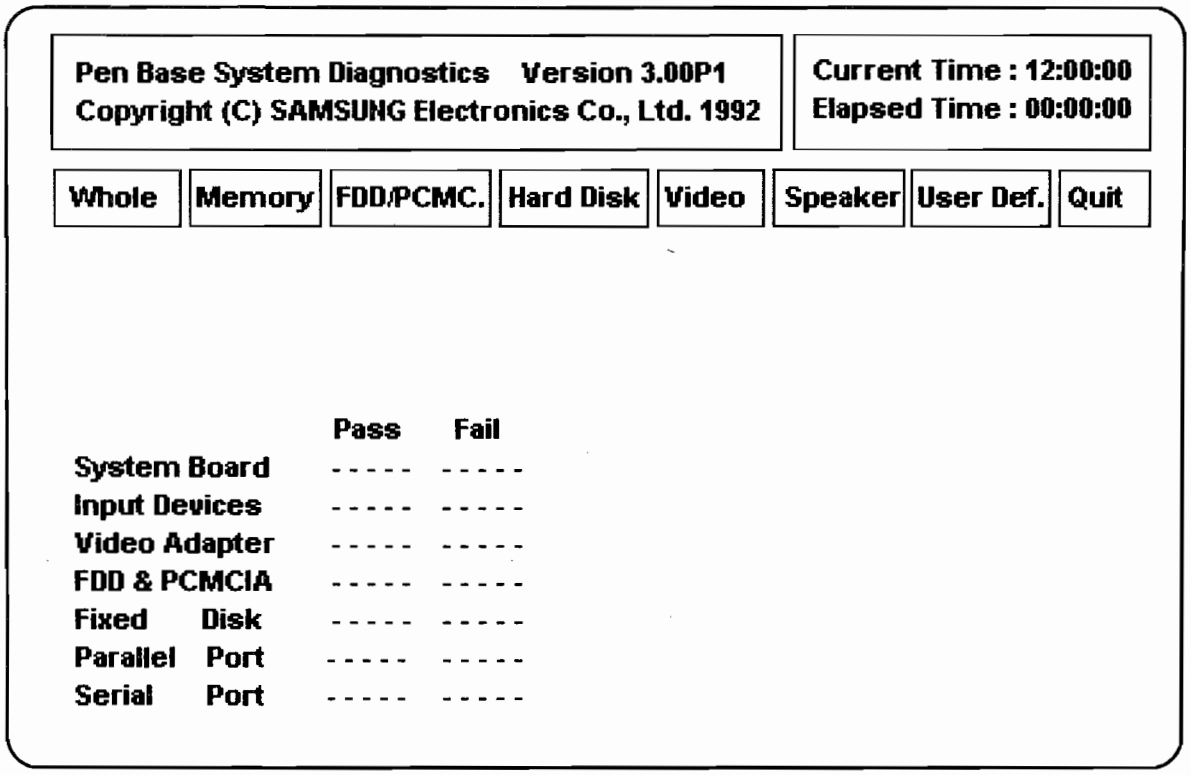


Figure 4-4. Automatic Test Menu

The following sections describe the tests availble for each automatic test selection.

Whole

Tests all functions of the system. The *Whole* selection performs all other automatic tests (Memory, Video, FDD & PCMC, Hard Disk, Speaker, SIO, PIO, KEYBD, and PENTEST).

Memory

Tests the Coprocessor, the BIOS ROM, additional system ROM, the I/O Adapter ROM, the Base/Extended RAM, and the CMOS RAM multiple times.

FDD/PCMC.

Tests the FDD Reset, the R/W test, the Seeking test, the Motor Spd, and the PCMCIA multiple times.

Hard Disk

Tests the HDD Reset, the R/W test, the ECC test, and the Seeking test multiple times.

Video

Tests the Text Mode, the Graphic Mode, the Alignment, and the Video RAM multiple times.

Speaker

Tests the speaker output, to 10 KHz

User Def.

Allows the user to define the order in which the tests are performed.

Quit

Returns to the main menu.

Running The Automatic Test

Once started, the automatic tests run continuously. You can stop the tests by pressing **Ctrl** + **C**.

When the *Whole* test calls another test, the called test is performed once, then the *Whole* test calls the next test in the order defined in KEYIN.DAT. The *Whole* test is the only test that can call other tests. You can specify the number of times a test is performed before the test starts.

The KEYIN.DAT file contains the order of the tests. If this file does not exist in the current directory, it will be created. You can also create the file using the *Init.* selection of the main menu.

Auto Edit

You can change the order of the automatic tests by selecting *Auto Edit* from the main menu. If you select *Auto Edit* and *Whole*, the Auto Edit screen is displayed (see Figure 4-5). You can add or delete test procedures by using the **Ins** and **Del** keys.

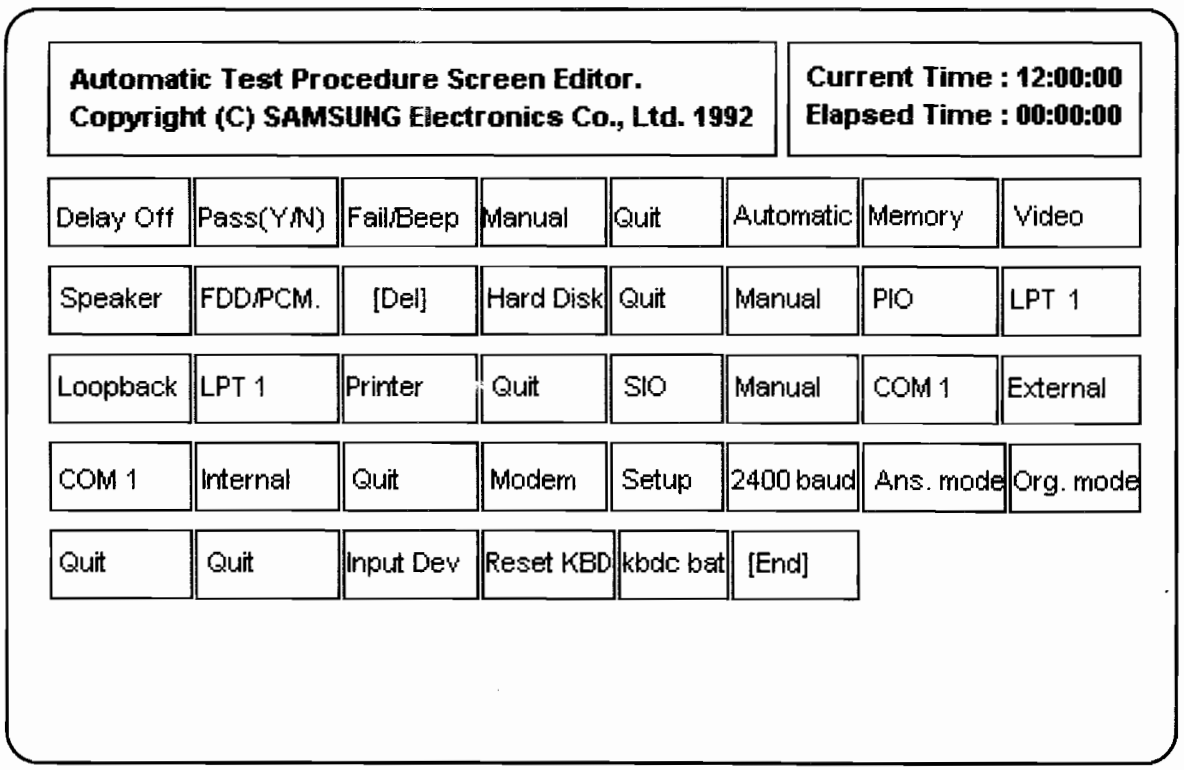


Figure 4-5. Auto Edit Screen

Structure of the Test Order

The test order can be defined as *Scan Code* order. The actual values of the function keys are **F1** = BBH ... **F8** = C2H. In the case of the *FDD/PCMC*, the actual test order is **F4** - **F1** -**F1** - **F8** - **F3** ..., etc. Figure 4-6 shows a flow chart of the test order.

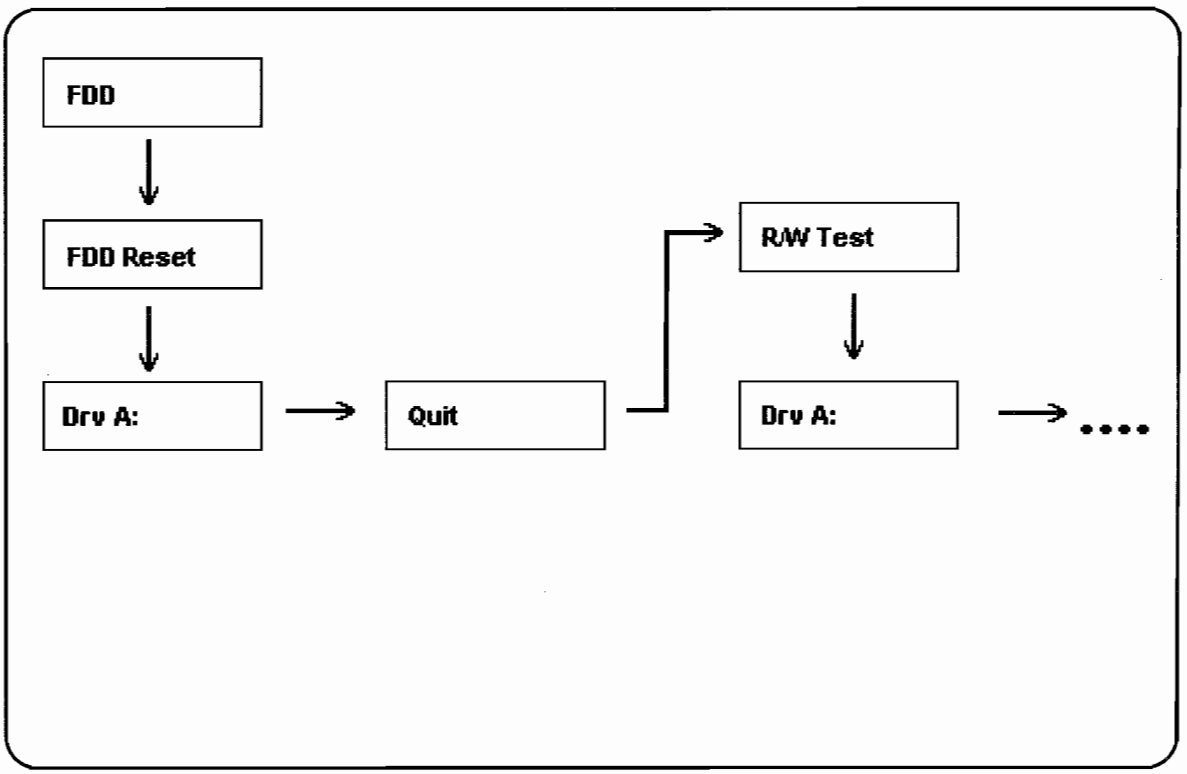


Figure 4-6. Flow Chart of the Test Order

When deleting or adding tests, the test order can change unexpectedly if the corresponding *Quit* is not deleted or added at the same time. Figure 4-7 shows the test order after deleting *FDD* but not deleting a corresponding *Quit*. In other words, you must delete a *Quit* whenever you delete a test from the order. Also, you must add a *Quit* whenever you add a test to the test order.

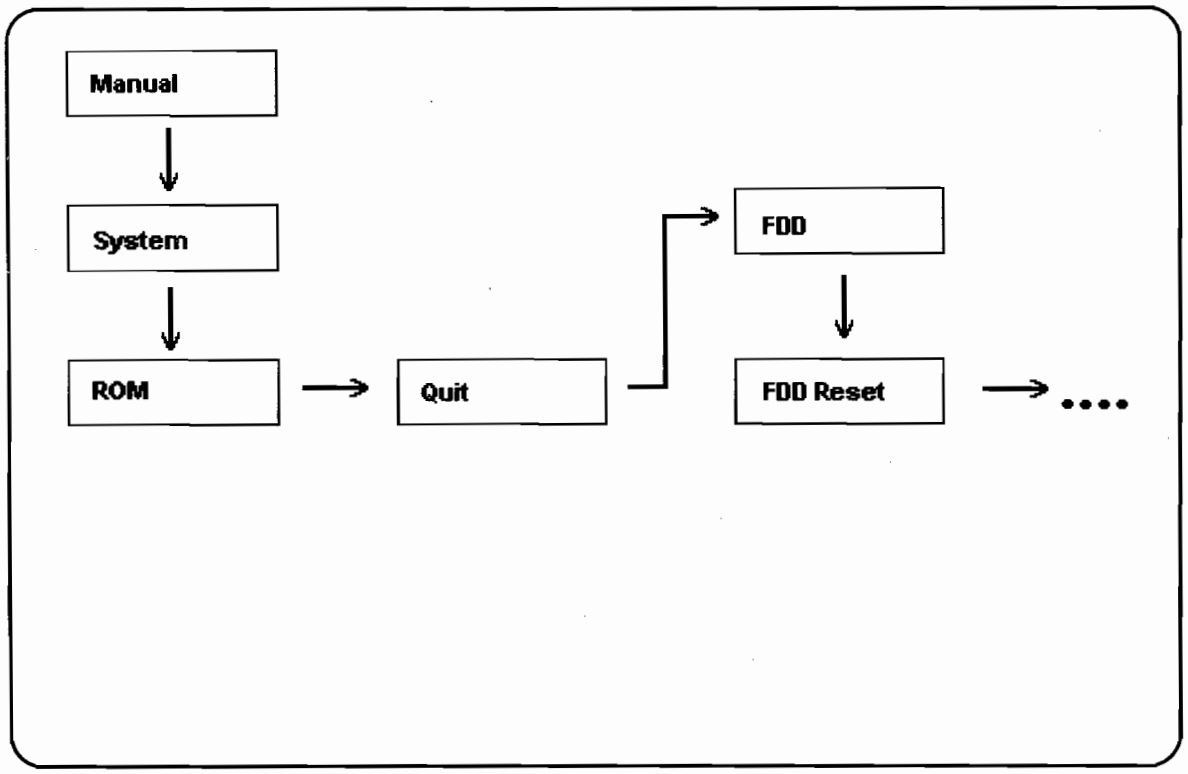


Figure 4-7. Flow Chart after Deleting FDD Test Only

Modifying the Test Order

To delete a test item, perform the steps that follow.

1. Move the cursor to the item to be deleted.
2. Press **Del** key.

To add a test item, perform the steps that follow.

1. Move the cursor to the location to be added.
2. Press **Ins** key; the "?" will be added.
3. Add the new test item.

To define the "?" selection, perform the steps that follow.

1. Move the cursor to the location to be defined.
2. Press the space bar; the cursor moves to the bottom of the screen.
3. Move the cursor to the item to be defined.
4. Press the space bar or the **Enter** key.

The **End** key is used in the system and can't be deleted; the **Del** key is used in the system and can be deleted.

Init.

The *Init.* selection of the main menu is used to create the data files. *ERROR.REC* is used to create the ERROR.REC file and *KEYIN.DAT* is used to create the KEYIN.DAT file. *Ext. Proc* is used to call and run external programs.

Large Fail

The *Large Fail* selection prevents the "Fail" message from being displayed.

Sys Info.

Sys Info. provides information about the system, such as the CPU type, coprocessor status, RAM and ROM size, HDD drive type, and information regarding the SIO, PIO, keyboard, and video adapter.

Disp Err.

The *Disp Err.* selection of the main menu is used to display the error messages that occured during the diagnostic tests.

Aging Off/Aging On

When you select this item, the aging mode is toggled between "On" and "Off." If the current mode is "On," the automatic test *Whole* is loaded once you load *LOADER.COM* without any user's input. You can use this option as a burn-in test by inserting *LOADER.COM* in the *AUTOEXEC.BAT* file. To turn the Aging mode "Off," press **Ctrl** + **C** to stop the automatic test, and select *Aging On* from the main menu.

Exit

The *Exit* selection of the main menu will finish the testing and exit to the DOS environment. Before running any applications, you should reset the system.

Error Messages

System

10	System RAM	0810: High Address Bus Short Error 0820h: Data Bus Short Error 0830h: Data Pattern R/W Error 0840h: Even/Odd Bank Access Error 0850h: Cell Test Data Error 0851h: Cell Test Address Error 080000h - 08FFFFh: Error Block in 64K Unit
11	Cache SRAM	08XX: Error Bit Set 0800h - 08FFh: Error Page Number
12	BIOS ROM	002Ch: Byte Checksum Error Value
13	Extended BIOS ROM: Byte Checksum Error Value - Socket on CPU board	
14	I/O Adapter ROM Checksum Error	
15	CMOS RAM R/W Error 21 04: 21 is Error Address (21h Register), 04 is Error Bit Set (0000 0100)	
16	Speaker Error 00 00: 00 00 does not have meaning	
17	Local Standby Test Error	
18	Global Standby Test Error	
19	S/W Generated SMI Test Error	
1B	80386SL/82360SL Chipset Error	
1C	NPX Transfer Test Error	
1D	NPX Divide by 0 Exception Test Error	
1E	NPX Mathematic Function Test Error	
1F	PMS Command Test Error	

Keyboard and Digitizer (Mouse)

20	Keyboard Processor Reset Error 00 0d: Received Code Other Than AAh
21	Keyboard Scancode Test Error 00 00: 00 00 Does Not Have Meaning
22	Keyboard BAT Test Error
23	Keyboard Handshake Test Error
24	Mouse Test Error
25	Digitizer Diagnostic Command Test Error
26	Digitizer Echo Back Command Test Error
27	Digitizer Request Version Test Error
28	Digitizer Calibration Test Error
29	Digitizer Line Drawing Error

Video Adapter

30	EGA/VGA General Error
31	Video RAM Test Error
32	Read Mode 0 Test Error
33	Read Mode 1 Test Error
34	Write Mode 0 Test Error
35	Write Mode 1 Test Error
36	Write Mode 2 Test Error
37	Write Mode 3 Test Error
38	Switch Setting Test Error
39	Reading Inactive Plane Test Error
3A	Reading Active Plane Test Error
3B	Rotation Function Test Error
3C	Linear Address Test A0 - A7 Error
3D	Linear Address Test A9 - A15 Error
3E	Cursor Address Test A0 - A7 Error
3F	Cursor Address Test A8 - A15 Error
40	Cursor Address Test A16 - A17 Error
41	Bit Mask Function Test Error
42	Latched Data Test Error
43	Even/Odd Mode Test Error
44	CRTC/TS/GDC/ATC Test Error
45	Internal REG Test Error
46	Ext Palette Short Test Error
47	Ext Palette R/W Test Test Error
48	Translation ROM Data Test Error
49	EGA/VGA Chip Diagnostics Error
50	Color Attribute Test Error
51	Character Set Test Error
52	80 x 25 Mode Test Error
53	40 x 25 Mode Test Error
54	80 x 60 Mode Test Error
55	320 x 200 Palette 0 Test Error
56	320 x 200 Palette 1 Test Error
57	640 x 200 2-Color Test Error
58	640 x 200 16-Color Test Error
59	640 x 350 16-Color Test Error

30	EGA/VGA General Error
5A	640 x 480 16-Color Test Error
5B	800 x 600 16-Color Test Error
5C	1024 x 768 16-Color Test Error
5D	320 x 200 256-Color Test Error
5E	640 x 480 256-Color Test Error
5F	8 Page Change Test Error
60	Text Scrolling Test Error
61	2 Font Display Test Error
62	8 Fonts Display Test Error
63	Panning/Split Screen Test Error
64	Smooth Scroll Test Error
65	Window/Zooming Test Error
66	100 x 50 16-Color Test error
67	720 x 512 16-Color Test Error
68	Video Display Test Error
69	VGA.EXE Load & Execute Error

Diskette Drive and PCMCIA

70	Reset Error d0 00:	d is Error Drive (0 /1)
71	Format Error 00 00:	00 00 Does Not have Meaning
72	R/W Test Error xx yy:	xxh = h00s ssss: s = Error Sector (1 - 12h), h = Error Head (0 / 1) yyH = dttt tttt: t = Error Track (0 - 4Fh), d: Error Drive (0 /1)
73	Seeking Error d0 tt:	tt = Error Track (0 - 4Fh), d = Error Drive (0 / 1)
74	Motor Speed Error d1 96:	196 = Time for One Ratation (s), d = Error Drive (0 /1)
76	FDD R/W Data Error	
77	PCMCIA initialization Test Error	
78	PCMCIA Device Test Error	
79	PCMCIA Device Information Test Error	

Hard Disk

80	Reset error d000 0000 0000 0000:	d = Error Drive (0 / 1)
81	Format Error dhhh h0tt tttt tttt:	t = Error Track (0 - 1023), h = Error Head (0 - 15), d = Error drive (0 /1)
82	R/W Test Error dhhh h0tt tttt tttt:	Same As Format Error
83	Seeking Error d000 00tt tttt tttt:	t = Error Track (0 - 1023), d = Error Drive (0 /1)
84	HDD ECC Test Error	

Printer Port

90	Data Port R/W Error 0p xx:	p = Error Port (0 /1), xx = 000a bcde; Error Pin Combination: a = (11) - (17), b = (10) - (16) c = (12) - (14), d = (01) - (13), e = (02) - (15)
91	Control Port R/W Error	0p xx: Same As Above
92	Loopback Test Error	0p xx: Same As Above
93	Interrupt Test Error	0p xx: 0p = Error Port (0 / 1), xx = Does Not Have Meaning
94	Printing Test Error	

Serial Port

A0	Loopback Test Error	
A1	Send/Receive Error	
A2	Modem Control Port Error	
A3	RxD INT Test Error 0pxx ssss:	ssss = Sent ASCII, 0p = Error Port (COM1/COM2), xx = No Meaning
A4	TxD INT Test Error 0pxx	ssss: Same As Above
A5	Break INT Test Error 0pxx	ssss: Same As Above
A6	DCD/CTS INT Test Error 0pxx	ssss: Same As Above
A7	DSR/RI INT Test Error 0pxx	ssss: Same As Above
A8	Overrun INT Test Error 0pxx	ssss: Same As Above
A9	Baud Test Error 0pxx	ssss: Same As Above
AA	Port Not Attached Error	
AB	Loopback Test Timeout Error	
AC	INT Test Timeout Error	

Modem

C0	Modem Status REG. Defective Error
C1	Not a Compatible Modem Error
C2	Modem Not Connected Error
C3	Modem CPU Command Mode Test Error
C4	Modem CPU Command Bus Test error
C5	Modem – UART Status Error
C6	Modem CPU Command Accept Error
C7	Originate Mode Carrier Test Error
C8	Answer Mode Carrier Test Error
C9	Modem Not Initialized Error
CA	Modem Not Installed Error

Loopback Connection Structure

Serial Loopback Connection

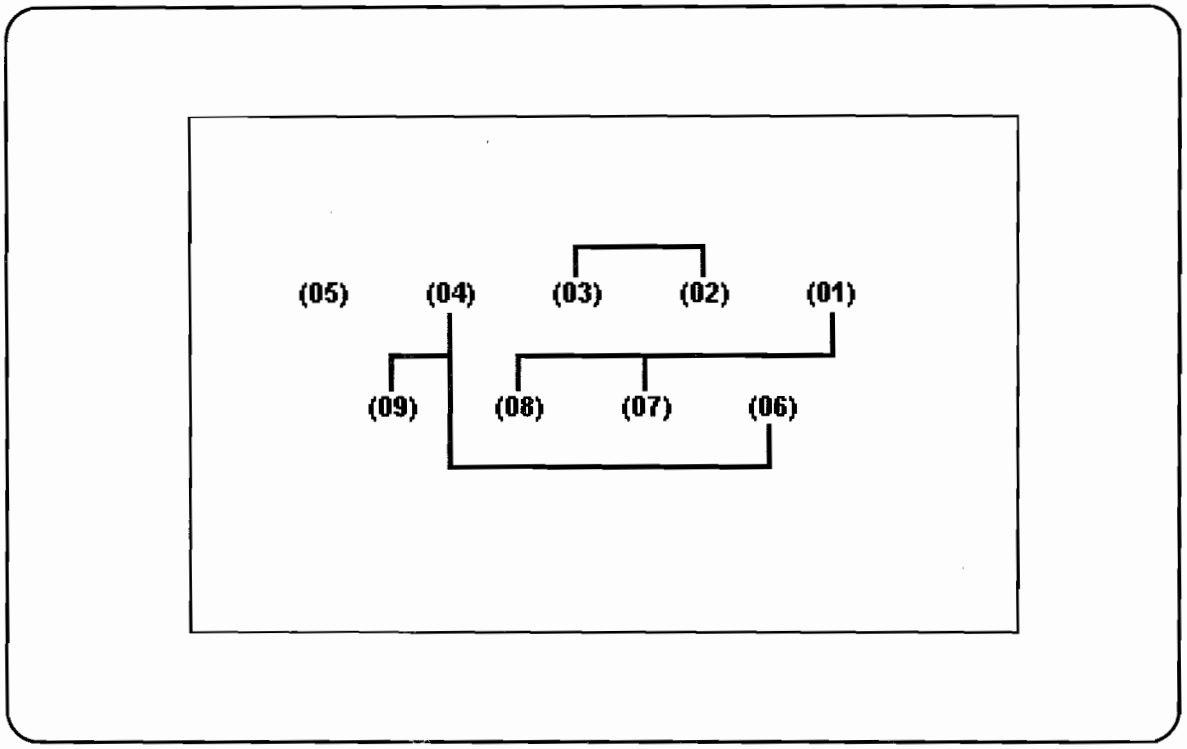


Figure 4-8. Serial Loopback Connection

Parallel Loopback Connection

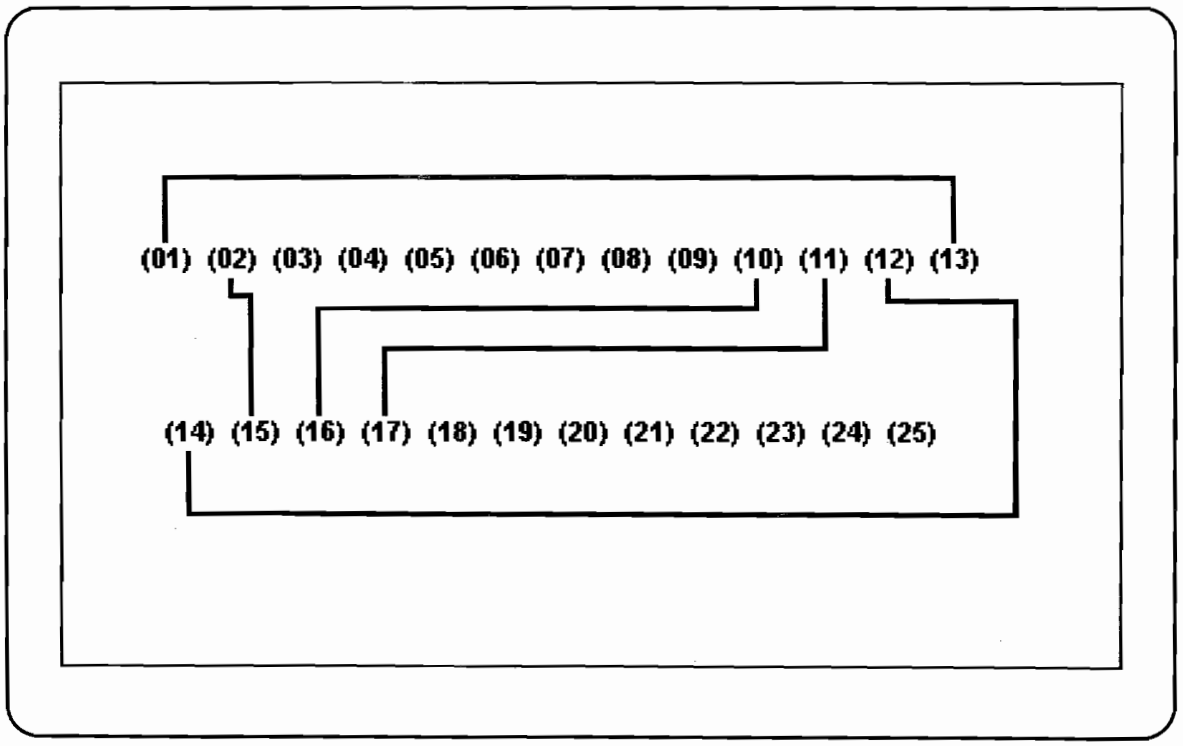


Figure 4-9. Parallel Loopback Connection

5. Principles of Operation

5 Principles of Operation

Contents

Tables

Introduction

This chapter provides an overview of the major devices used in this system. No attempt is made to duplicate the components' specification sheets.

Please refer to publication referral section to locate the appropriate manual for your needs.

Intel386 SL SuperSet

Overview

The Intel386 SL Microprocessor SuperSet is an extremely flexible pair of components marking a new milestone in microcomputer technology. Included in the pair are an Intel386 Architecture Central Processing Unit (CPU), a memory subsystem controller capable of controlling either DRAM or SRAM, address translation and remapping logic, a cache memory controller, and an extensive collection of ISA bus compatible peripheral functions.

The SL SuperSet allows the personal computer designer to take advantage of the highest level of system integration, while preserving complete freedom in selecting system features, power/performance trade-offs, and value-added enhancements.

Essentially, all of the components needed to build an ISA bus compatible personal computer have been combined within just two components: the Intel386 SL Microprocessor and memory control system, and the 82360SL ISA peripheral I/O and power management subsystem. The only other components needed for a complete personal computer are the main DRAM or optional static memory subsystem, optional cache SRAM and a graphics controller. A minimal amount of commodity Small Scale Integration (SSI) logic or Medium Scale Integration (MSI) logic buffers may be required for design-specific interface to peripheral devices on the ISA bus.

Functions and features of the two SL components are given in Tables 5-1 and 5-2. Detailed descriptions are given in the sections that follow.

Table 5-1. Intel386 SL Microprocessor Functions and Features

Function	Features
Static Intel386 CPU Core	Optimized and Compatible with Standard Operating System Software such as: MS-DOS, WINDOWS, OS/2, and UNIX; Object Code compatible with Intel 8086, 80286 and Intel386 Microprocessors; Runs all desk-top applications 16- or 32-bit; DC to 25 MHz operation; 20 MB physical memory/64 TB virtual memory; 4 GB maximum segment size; High-integration, low-power Intel CHMOS IV process technology.
Transparent Power-Management System Architecture	System management mode architecture extension for truly compatible systems; Power management transparent to operating systems and application programs; Programmable hardware supports custom power-control methods.
Direct Drive Bus Interfaces	Full ISA bus interface, with 24 mA drive; High-speed peripheral interface bus
Integrated Cache Controller and Tag RAM	No-glue cache SRAM interface; 16, 32, or 64 KB cache size; Direct, 2-way or 4-way set associative organization; Write posting-posted memory writes; 16-bit line size — reduces bus utilization for cache line fills; Write-thru, with SmartHit algorithm for reduced main memory power consumption.
Programmable Memory Control	No-glue, page-mode DRAM interface; SRAM support for lowest power; 1, 2, or 4 banks interleaved, with programmable wait states; 512 KB to 20 MB; Advanced, flexible address-map configuration; Full hardware LIM EMS 4.0 address translation to 32 MB without wait-state penalty.

Table 5-2. 82360SL I/O Subsystem Functions and Features

Function	Features
Complete ISA System, with extended support	Full ISA bus control, status and address and data interface logic, with full 24 mA drive; Compatible ISA bus peripherals: Two 8237 direct memory access controllers; Two 8254 programmable timer counters (6 timer/counter channels); Two 8259A programmable interrupt controllers (15 channels); Enhanced LS612 page memory mapper; 146818-compatible real-time clock w/256-bytes CMOS RAM; Two 16450-compatible serial port controllers; 8-bit parallel I/O port with high-speed protocol (centronics or bi-directional). Additional System I/O decoding, programmable chip selects and support interfaces: Full Integrated Drive Electronics (IDE) hard disk interface; Floppy disk controller; Keyboard controller chip selects and support logic. External real-time-clock support; PS/2 and EISA control/status ports; Local memory and ISA-bus memory refresh control; New ideaport interface for hardware expansion.
Transparent Power-Management System Architecture	Architecture extension for truly compatible systems; Transparent to operating systems and applications programs; Programmable hardware supports custom power-control methods; Integrated power-management unit manages power events safely

Intel386 SL Microprocessor: CPU and Memory-Controller Subsystem

The Intel386 SL Microprocessor is a highly-integrated, complete microprocessor and memory controller subsystem. At the heart of the Intel386 SL Microprocessor is a CHMOS static Intel386 CPU core. The Intel386 CPU core has been fully optimized to reduce run-time power requirements, and includes a key architectural extension required by battery-operated systems.

The Intel386 SL processor is the first member of the Intel386 Microprocessor product line to implement a CPU with the System Management Mode extension. The System Management Mode is a new CPU operating-mode which allows system vendors to rid their systems of the backwards-compatibility problems that plague battery-operated PCs. This Intel386 architecture extension eliminates portable-system conflicts by providing a safe, new operating level for the battery management firmware developed by system designers. With the Intel386 SL CPU, firmware will execute transparently to every application, operating system and CPU mode, thus avoiding the compatibility conflicts which were once unavoidable.

The Intel386 SL Microprocessor retains the paged-memory-management system, and all other key features which are common to the Intel386 architecture. In addition, on-chip hardware implements the Expanded Memory Specification (E.M.S.) address translation compatible with the current Lotus/Intel/Microsoft (L.I.M.) E.M.S. 4.0 standard. Additional address-mapping and control logic integrated in the Intel386 SL CPU allows BIOS ROMs to be "shadowed" by faster memory devices, and supports a variety of common memory roll-over and back-fill schemes. The Intel386 SL CPU contains all of the control and interface logic needed to directly drive large main memory and an optional cache memory subsystem.

The Intel386 SL CPU contains bus drivers and control circuitry for two expansion interfaces. A Peripheral Interface Bus (PI-Bus) provides high-speed communication with fast devices such as VGA and FLASH Disk. The Industry Standard Architecture (ISA) bus provides a common interface for the wealth of third party ISA bus compatible I/O peripheral and expansion memory add-in boards. On-chip data-byte steering logic, address decoding and mapping logic automatically routes each memory or I/O operation to the appropriate local memory, cache, PI-Bus or ISA expansion bus.

All system configuration logic in the Intel386 SL processor subsystem is initialized under software control.

The system designer only has to program the processor in order to support multiple system hardware designs where many devices of less flexibility were once required. System characteristics such as memory type, size, speed, organization, and mapping; cache size, organization and mapping; and peripheral selection, configuration and mapping are configured under software control. Thereafter, all memory and I/O transfer requests are automatically sent to the appropriate memory space or expansion bus, fully-transparent to existing operating system software and application programs.

82360SL I/O: Integrated ISA Peripheral and Power-Management Device

The 82360SL Peripheral I/O contains dedicated logic to perform a number of CPU, memory, and peripheral support functions. The 82360SL device also contains an extensive set of programmable power management facilities which allow minimized system energy requirements for battery-powered portable computers.

The 82360SL includes a complete set of one-chip peripheral device functions including two 16450 compatible serial ports, one 8-bit Centronics interface or bi-directional parallel port, two 8254 compatible timer counters, two 8259 compatible interrupt controllers, two 8237 compatible DMA controllers, one 74LS612 compatible DMA page register, one 146818 compatible Real-time clock/calendar with an additional 128 bytes of battery backed CMOS RAM and an integrated drive electronics (IDE) hard disk drive interface. The Intel 82360SL also contains highly programmable chip selects and complete peripheral interface logic for direct kçboard and floppy disk controller support. The peripheral registers and functions behave exactly as the discrete components commonly found in industry standard personal computers. The peripheral logic is enhanced for static operation by supporting write only registers as read/write.

The processor and memory support functions contained in the 82360SL device eliminate most of the external random-logic "glue" that might otherwise be required. The 82360SL device provides internal programmable-frequency clock generators for the ISA bus backplane, and video subsystems. A programmable, low-power DRAM refresh timer is also provided to maintain system memory integrity during the power saving suspend state.

The 82360SL also contains a flexible set of hardware functions to support the growing sophistication in power management schemes required by portable systems. Numerous hardware timers, event monitors and I/O interfaces can programmably monitor and control system activity. Firmware developed by the system designer allocates and directs the hardware to fulfill the unique power management needs of a given system configuration.

All of the standard peripheral registers, clock-generation logic, and power-management facilities have been designed to ensure complete compatibility with existing operating systems and applications software.

External Memory Arrays

The Intel386 SL processor hooks directly to either SRAM or DRAM memory devices with total capacity from 512 Kilobytes to 20 megabytes, with optional parity. Depending on the type and size of the memory devices involved, control logic generates the appropriate chip-select, bank-select, byte-enable, and read and write control signals.

The Intel386 SL processor also contains control logic for a smaller, optional memory array. The internal control unit includes the tag bits and comparators needed for a variety of cache sizes and configurations. The cache interface requires no "glue": separate, dedicated pins drive all cache address and data buses and generate all chip-select and byte-enable control signals, so external cache systems consist of just one, two, or four memory components.

The "BIOS Memory" includes ROM, EPROM, or Flash EPROM memory devices that hold the basic I/O system software for ISA computers. The same array may also contain system-specific initialization and configuration software, and may contain interrupt and trap-handler routines used for power-management software.

The SL SuperSet supports two additional optional memory arrays for special system functions. The "Flash Disk Emulator" block contains non-volatile memory devices used to replace or augment conventional disks and diskette drives with a solid-state file-storage system. This memory can be arbitrarily large, and can hold OS code, application programs, and important data files indefinitely, even with all power removed from the system.

The optional memory called "System Management Memory" holds code and data needed by supervisory system functions, information that would normally be concealed from OS and application programs. Portions of this memory may be implemented with Flash EPROMs or micro-power static RAMs, in which case critical system status information can be retained when power to the rest of the computer is disabled. With the proper software, this facility lets the computer power itself down when idle, and later resume program execution automatically at the exact point it ceased.

System Interconnect Buses

The various pins on the SL SuperSet components generally connect to corresponding pins on other components, external memory arrays, peripherals, or the expansion bus. Certain pins supply the clock signal inputs to each device and support the various power management functions. Others pass control and status information between chips and supply pre-decoded chip-select signals, eliminating external random-logic "glue".

All signal pins that connect to the bus called "ISA System Backplane" can drive directly up to eight standard expansion slots. These include 24-bit system and local address (SA and LA) buses and a 16-bit system data (SD) bus. A control bus supervises memory and I/O read and write operations and services requests for interrupts and direct-memory-access (DMA) transfers. Table 5-3 summarizes the SL SuperSet pins that attach directly to the ISA backplane connectors.

Table 5-3. SL SuperSet Expansion-Bus Pins Directly Drive the ISA Backplane

i386SL	82360SL	Signal Mnemonic	Signal Function
X	X	SD15:0	System Data Bus
X		SA19:17	System Address Bus
X	X	SA16:0	System Address Bus
X	X	LA23:17	Local Address Bus
	X	SMEMW#	System Memory Write
	X	SMEMR#	System Memory Read
X	X	MEMW#	Memory Write
X	X	MEMR#	Memory Read
X	X	IOW#	I/O Port Write
X	X	IOR#	I/O Port Read
	X	AEN	System Address Enable
	X	IRQ15:10, 8:3,1	System Backplane Interrupt Requests
X	X	IRQ9	VGA Interrupt Request
	X	DRQ7:5,3:0	Direct Memory Access Requests
	X	DACK7:5,3:0	Direct Memory Access Acknowledge
X	X	SBHE#	System Bus High Enable
	X	TC	Terminal DMA Transfer Cycle Count
X	X	IOCHRDY	I/O Channel Ready
X	X	OWS#	Zero Wait-State Transfer
	X	REFRESH#	System-Memory Refresh Cycle
X	X	MASTER#	AT Bus Master
X	X	BALE	Buffered Address Latch Enable
	X	RESETDRV	Cold System Reset
	X	OSC	System-Bus Oscillator
X		MEMCS16#	16-Bit Mem Transfer Mode Chip Select
X	X	IOCS16#	16-Bit I/O Transfer Mode Chip Select
	X	IOCHCHK#	I/O Channel Check
X	X	SYSCLK	System Clock

Main Memory Options

The Intel386 SL processor contains control and interface logic for main memory arrays built with either static (SRAM) or dynamic (DRAM) memory devices, with or without parity. The address and control functions performed by Intel386 SL processor pins vary, depending on the memory type selected. Address signals can be either latched or multiplexed, and control outputs can provide bank-select, chip-select, and byte-enable signals as appropriate for the sizes of memory components currently installed. DRAM refresh sequencing and parity generation and verification (if enabled) are automatic.

DRAM Main Memory

High-capacity main-memory arrays generally require fewer chips when built using DRAM devices. The DRAM control logic built into the Intel386 SL processor is extremely flexible. DRAM arrays can be 16 or 18 bits wide depending on whether automatic parity verification is enabled. Dedicated RAS#, CAS#, and WE# strobes are provided separately for the high- and low-order bytes for each DRAM bank.

The DRAM controller supports three different memory speeds. The number of CPU cycles allotted to each transfer varies to compensate for different CPU frequencies and memory speeds. One, two, three or four banks may be installed at a time. With two or four banks installed, accesses are interleaved between banks one and two, three and four for higher transfer rates.

With four banks installed, each pair may be a different size, allowing a range of memory configurations with total capacity from 512K to 20M bytes. Pins MA 10:0 multiplex different sets of address bits according to the number of DRAM banks installed and the size and interleave mode of the components in each bank.

A number of special Intel386 SL processor facilities reduce DRAM power consumption. Only the memory devices involved in each transfer are enabled. With page-mode DRAMs, successive transfers within the same page produce CAS#-only transfer cycles for greater speed and reduced lower power. The refresh rate is programmable, and the controller can perform CAS# before RAS# refresh sequencing to reduce power-supply transients ("spiking"), improve performance, and increase power efficiency.

Memory System Sizing and Control Mechanisms

The characteristics of the main memory controller, including the type and operating mode of the devices used, the number of the installed banks, and the size of each bank are configured through software at initialization time. System initialization software can test the size and characteristics of memory components currently installed and dynamically adjust memory-control algorithms according to the results of those tests. A number of control pins alter their function depending on the basic memory technology selected; the alternate functions performed by each of these pins is shown in Table 5-4. For further details, consult the *Intel386 SL Microprocessor SuperSet Programmer's Reference Manual.*

Table 5-4. Intel SL SuperSet Multifunction Main Memory Control Signals

Signal Mnemonic	DRAM-Mode Pin Function	SRAM-Mode Pin Function
CMUX0	CAS, Low Byte, Bank 3	Transceiver Direction
CMUX1	CAS, High Byte, Bank 3	Address Latch Enable
CMUX2	CAS, Low Byte, Bank 2	Transceiver Enable, Bank 3
CMUX3	CAS, High Byte, Bank 2	Transceiver Enable, Bank 2
CMUX4	CAS, Low Byte, Bank 1	Transceiver Enable, Bank 1
CMUX5	CAS, High Byte, Bank 1	Transceiver Enable, Bank 1
CMUX6	CAS, Low Byte, Bank 0	Transceiver Enable, Bank 0
CMUX7	CAS, High Byte, Bank 0	Transceiver Enable, Bank 0
CMUX8	RAS, Bank 3	Chip Enable, Bank 3
CMUX9	RAS, Bank 2	Chip Enable, Bank 2
CMUX10	RAS, Bank 1	Chip Enable, Bank 1
CMUX11	RAS, Bank 0	Chip Enable, Bank 0
CMUX12	Low-Order Byte Parity Error	Low-Byte Output Enable
CMUX13	High-Order Byte Parity Error	High-Byte Output Enable

Cache Memory System

High-performance computers traditionally include cache memory to reduce main memory latency and boost system throughput, albeit at the expense of increased system complexity and power requirements. The optional high-speed cache system supported by the SL SuperSet allows the simplest possible implementation, and can both improve CPU performance and reduce system power consumption.

The Intel386 SL processor drives the cache memory components directly through separate, dedicated address, data, and control buses, eliminating all external glue. The only components needed to add cache to a SL SuperSet-based system are the memory devices themselves, potentially just a single external SRAM. Control logic built into the Intel386 SL processor remaps the cache memory to support different cache sizes and organizations, and includes address, status, and tag bits and comparators for each.

Configuration Options

The Intel386 SL processor supports cache configurations with capacities of 16K, 32K, or 64K bytes, using just one, two, or four external SRAMs. Address bus CA15:0 directly drives the address inputs of each SRAM, and data bus CD15:0 connects directly to the SRAM data pins. Dedicated write-enable and output-enable signals for the cache (CWE# and COE#) drive the SRAM control inputs directly. Separate chip-select outputs (CCHE# and CCLE#) enable the high- and low-order cache bytes.

Each cache line is two bytes wide, and each set of tag bits controls a block of 16 cache lines. The cache controller contains 2048 sets of tag bits, which may be programmed to form any of the three organizations. The simplest (direct-mapped) organization arranges the tags as a single linear array, in which case each address in the main memory space corresponds directly to a single cache location.

Tags may also be grouped into two banks of 1024 tags (two-way set-associative) or four banks of 512 tags (four-way set associative), in which case each main memory address can map onto any of several locations within the cache. Direct, two-way or four-way associativity can be achieved with any number of cache memory chips.

When a cache miss occurs, control logic uses a least-recently used (LRU) algorithm to determine which cache block to replace with more recent data. The cache always operates in write-through mode, i.e., main memory is also updated whenever the CPU writes new data to the cache. This assures the main memory will always match updated data in the cache, and assures full compatibility with existing system software and hardware.

Cache Performance Factors

Cache memory affects the performance of several typical PC configurations executing the 32-bit Dhrystone benchmark program. The "Theoretical Maximum Performance" is defined as the level that would be achieved by an "ideal" Intel386SX CPU-based computer, i.e., one whose entire main memory is built with non-pipelined zero-wait-state memory devices for CPU speeds up to 20 MHz. Conventional (cacheless) DRAM systems typically incur an average of 0.8 wait states per memory access, which lowers performance to about 80% of the theoretical maximum.

Memory control logic in conventional PCs cannot begin a new transfer until its intended destination is known, which is not until the target address appears on the CPU address pins. With the Intel386 SL Processor, however, the DRAM control logic is part of the CPU. Information about successive transfers is known before their addresses leave the part, which lets the SL SuperSet implement control algorithms that are considerably more sophisticated than those possible with discrete DRAM controllers. Page-mode data transfers and memory-bank interleaving eliminate unnecessary recharge cycles, so the performance of a cacheless SL SuperSet-based PC with 80-ns DRAMs is close to 90% of the theoretical maximum. Adding cache boosts this figure to about 94%.

While the SRAMs used as cache memories are relatively small but quite fast, those used for personal computer main memories are typically larger, slower, and use less power than their DRAM counterparts. A SRAM-based Intel386 SL processor system with no cache might typically insert three wait states into each transfer, which reduces performs to about one-third the potential maximum rate. A cache eliminates most of these wait states. Adding a cache therefore improves the performance of SRAM-based PCs dramatically, and effectively boosts throughput to the same level as considerably faster DRAMs.

Conventional PC caches generally increase system power requirements by the amount consumed by the control logic and cache components themselves. Adding cache to an Intel386 SL Microprocessor system, on the other hand, can actually reduce system power.

The Intel386 SL Processor's internal cache controller implements a SmartHit control algorithm that pipelines tag look-ups with data retrieval. Tag bits determine whether a memory request will hit within the cache array in time to prevent unnecessary transfers to main memory. Only the necessary cache operation completes. Conversely, the SmartHit control logic knows when a cache miss occurs early enough to initiate a main-memory or expansion-bus transfer, as needed, without further delay.

The power consumed by DRAM memory systems is proportional to the number of transfer cycles they must perform. Since a cache subsystem satisfies the majority of all memory requests, adding cache eliminates most main memory access cycles. SRAM uses significantly less power per transfer cycle than DRAM, so the system power saved by eliminating DRAM transfers more than offsets the added load of the cache components.

The power consumed by SRAM-based main memories, on the other hand, is already quite low. In such designs the power savings attributable to cache is slight, but does help offset the power consumed by the cache memories. When conventional memory accesses must be performed, however, control logic disables the cache components to further reduce power.

System initialization software determines whether or not the cache system is enabled. The size of the external cache array and the set-associativity options are also set under software control.

BIOS Memory Array

The Intel386 SL processor directly generates control signals to enable a ROM, EPROM, or Flash EPROM array to hold basic I/O system (BIOS) and/or ROM-based system software. Depending on configuration options selected at initialization time, the BIOS memory array can be either 8 or 16 bits wide, and up to 128 Kilobytes long; arbitrarily large EPROM arrays can be supported with external decode logic. The processor generates special control signals to enable Flash memory reprogramming, so customized or updated versions of the BIOS can be downloaded after a system has been manufactured or sold.

Since ROMs and EPROMs are available at a variety of price/performance points, the BIOS control logic automatically inserts 0 to 15 wait states within each access cycle. A number of features increase the density, flexibility, or effective performance of the BIOS memory array. BIOS memory can be shadowed in much faster main memory, and VGA subsystem can be combined with the main system BIOS, lowering chip count and complexity.

Flash Memory Support

The Flash EPROM array is accessed through the same address and data bus as the ISA expansion interface, but with separate, dedicated control lines. For expanded memory access, remapping hardware divides the entire array into a collection of 64K-byte "windows" accessed through a reconfigurable block of memory addresses in the low-order megabyte of the system address space.

Flash EPROM devices can occupy any portion of the Intel386 SL Microprocessor's 32-megabyte physical memory space not filled with conventional memory. With external bank-switching logic, the Flash array can be arbitrarily large.

Guaranteed Compatibility

Each Intel386 SL Microprocessor SuperSet component complies with all industry-standard PC design conventions. Extensions to the basic CPU architecture provide facilities for configuring system hardware, switching modes, and managing system power consumption, totally transparent to existing software. The new System Management Mode provides a new, dedicated interrupt vector and a new control instruction for supervisory control and power management functions. Software and data structures needed to support these functions all reside in a memory partition that is inaccessible to conventional software. Unlike conventional design approaches, SL SuperSet-based systems do not depend on "terminate and stay resident" (TSR) routines that can interfere with existing application programs.

While the SL SuperSet includes a number of new capabilities for power-reduction, each circumvents the hazards found in conventional design techniques. Each new capability is supported by an extension to the basic Intel386 architecture, rather than by appropriating some aspect of the original architecture that may or may not be needed for a particular piece of software. All of the resources of the original 8086, 80286, and Intel386 Family processors are thus preserved intact, ensuring full compatibility with all existing application programs and operating systems.

Systems built with these products can therefore be made fully compatible at both the hardware and software levels with all existing business and scientific applications programs developed for the 8086, 80286, and Intel386 Family microprocessors and all of the 8086 and Intel386 Microprocessor operating systems now in use, including MS-DOS, OS/2, Windows 3.0, Windows-386, and UNIX System V.

Related Publications

This manual gives only a glimpse of the architecture and peripheral capabilities of the Intel386 SL Microprocessor SuperSet, and makes no attempt to describe its underlying instruction set, electrical specifications, or timing parameters. For design information of this type, consult th following related publications:

Intel386 SL Microprocessor SuperSet System Design Guide, Intel Order No. 240816

Intel386 SL Microprocessor SuperSet Programmer's Reference Manual, Intel Order No. 240815

Intel386 SL Microprocessor SuperSet Data Sheet, Intel Order No. 240814

Intel386 SL Microprocessor Software Writer's Guide, Intel Order No. 231499

82077AA CHMOS Single-Chip Floppy Disk Controller

Introduction

The 82077AA is a true single-chip floppy disk, and tape drive controller for the PC-AT and PS/2. The 82077AA, a 24 MHz crystal, a resistor package and a chip select implement a complete design. All drive control signals are fully decoded and have 40 mA drive buffers with selectable polarity. Signals returned from the drive are sent through on-chip input buffers with hysteresis for noise immunity. The integrated analog data separator needs no external compensation yet allows for a wide motor speed variation with exceptionally low soft error rates. The microprocessor interface has a 12 mA drive buffer on the data bus plus 100% hardware register compatibility for PC-AT's and PS/2's. Features of the 82077AA controller include:

- single-chip floppy disk solution
  - 100% PC AT compatible
  - 100% PS/2 compatible
  - 100% PS/2 Model 30 compatible
  - integrated drive and data bus buffers
- integrated analog data separator
  - 250 Kbits/sec
  - 300 Kbits/sec
  - 500 Kbits/sec
  - 1 Mbits/sec
- high-speed processor interface
- perpendicular recording support
- integrated tape drive support
- 12 mA host interface drivers, 40 mA disk drivers
- four fully decoded drive select and motor signals
- programmable write precompensation delays
- addresses 256 tracks directly, supports unlimited tracks
- 16 byte FIFO
- 68-pin PLCC package

Upon reset, (Pin 32) the 82077AA defaults to 8272A functionality. New features are either selected via hardware straps or new commands.

The 24 MHz clock can be supplied either by a crystal or a MOS level square wave. All internal timings are referenced to this clock or a scaled count which is data rate dependent.

The crystal oscillator must be allowed to run for 10 ms after VCC has reached 4.5V or exiting the POWERDOWN mode to guaranteed that it is stable.

Table 5-5. 82077AA Crystal Specifications

Parameter	Specificaton
Frequency	24 MHz ± 0.1%
Mode	Parallel Resonant Fundamental Mode
Series Resistance	Less than 40 Ω
Shunt Capacitance	Less than 5 pF

Microprocessor Interface

The interface consists of the standard asynchronous signals: RD, WR, CS, A0-A3, INT, DMA control and a data bus. The address lines select between configuration registers, the FIFO and control/status registers. This interface can be switched between PC AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC-AT.

Status, Data, and Control Registers

The base address range is supplied via the CS pin. For PC-AT or PS/2 designs this would be 3F0 Hex to 3F7 Hex.

Table 5-6. 82077AA Status, Data and Control Registers

A2	A1	A0	Type	Register	Mnemonic
0	0	0	R	Status Register A	SRA
0	0	1	R	Status Register B	SRB
0	1	0	R/W	Digital Output Register	DOR
0	1	1	R/W	Tape Drive Register	TSR
1	0	0	R	Main Status Register	MSR
1	0	0	W	Data Rate Select Register	DSR
1	0	1	R/W	Data (FIFO)	FIFO
1	1	0		Reserved	
1	1	1	R	Digital Input Register	DIR
1	1	1	W	Configuration Control Register	CCR

Reset

There are three sources of reset on the 82077AA; the RESET pin, a reset generated via a bit in the DOR and a reset generated via a bit in the DSR. All resets take the 82077AA out of the power down state.

On entering the reset state, all operations are terminated and the 82077AA enters an idle state. Activating reset while a disk write activity is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, and the 82077AA waits for a new command. Drive polling will start unless disabled by a new CONFIGURE command.

RESET Pin ("Hardware") Reset

The RESET pin is a global reset and clears all registers except those programmed by the SPECIFY command. The DOR Reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs DSR Reset ("Software" Reset)

These two resets are functionally the same. The DSR Reset is included to maintain 82072 compatibility. Both will reset the 8272 core which affects drive status information. The FIFO circuits will also be reset if the LOCK bit is a "0". The DSR Reset clears itself automatically while the DOR Reset requires the host to manually clear it. DOR Reset has precedence over the DSR Reset. The DOR Reset is set automatically upon a pin RESET. The user must manually clear this reset bit in the DOR to exit the reset state.

DMA Transfers

DMA transfers are enabled with the SPECIFY command and are initiated by the 82077AA by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting DACK and addresses need not be valid.

Drive Interface

The 82077AA has integrated all of the logic needed to interface to a floppy disk or tape drives which use floppy interface. All drive outputs have 40 mA drive capability and all inputs use a receive buffer with hysteresis. The internal analog data separator requires no external components, yet allows for an extremely wide capture range with high levels of read-data jitter, and ISV. The designer needs only to run the 82077AA disk drive signals to the disk or tape drive connector.

Cable Interface

The INVERT pin selects between using the internal buffers on the 82077AA or user supplied inverting buffers. INVERT pulled to VCC disables the internal buffers; pulled to ground will enable them. There is no need to use external buffers with the 82077AA in typical PC applications.

The polarity of the DENSEL pin is controlled through the IDENT pin, after hardware reset. For 5.25-inch drives a high on DENSEL tells the drive that either the 500 Kbps or 1 Mbps data rate is selected. for some 3.5-inch drives the polarity of DENSEL changes to a low for high data rates. Additionally, the two types of drives have different electrical interfaces. Generally, the 5.25-inch drive uses open collector drivers and the 3.5-inch drives (as used on PS/2) use totem-pole drivers. The output buffers on the 82077AA do not change between open collector or totem-pole, they are always totem-pole.

Controller Phases

For simplicity, command handling in the 82077AA can be divided into three phases: Command, Execution and Result. Each phase is described in the following sections.

Command Phase

After a reset, the 82077AA enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the 82077AA before the command phase is complete. These bytes of data must be transferred in the order prescribed.

82077AA CHMOS Single-Chip Floppy Disk Controller

Before writing to the 82077AA, the host must examine the RQM and DIO bits of the Main Status Register. RQM, DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the 82077AA after each write cycle until the received byte is processed. The 82077AA asserts RQM again to request each parameter byte of the command, unless na illegal command condition is detected. After the last parameter byte is received, RQM remains "0", and the 82077AA automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to retain compatibility with the 8272A, and to provide for the proper handling of the "Invalid Command" condition.

Execution Phase

All data transfers to or from the 82077AA occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the SPECIFY command.

Each data byte is transferred by an INT or DRQ depending on the DMA mode. The CONFIGURE command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions <threshold> is defined as the number of bytes available to the 82077AA when service is requested from the host, and ranges from 1 to 16. The parameter FIFOTHR which the user programs is one less, and ranges from 0 to 15.

A low threshold value (i.e., 2) results in longer periods of time between service requests, but requires faster servicing of the request, for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e., 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode, Transfers from the FIFO to the Host

The INT pin and RQM bits in the Main Status Register are activated when the FIFO contains (16-<threshold>)bytes, or the last bytes of a full sector transfer have been placed in the FIFO. The INT pin can be used for interrupt driven systems and RQM can be used for polled systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The 82077AA will deactivate the INT pin and RQM bit when the FIFO becomes empty.

Non-DMA Mode, Transfers from the Host to the FIFO

The INT pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The INT pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The INT pin will also be deactivated if TC and DACK# both go inactive. The 82077AA enters the result phase after the last byte is taken by the 82077AA from the FIFO (i.e., FIFO empty condition).

DMA Mode, Transfers from the FIFO To the Host

The 82077AA activates the DRQ pin when the FIFO contains (16-<threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The 82077AA will deactivate the DRQ pin when the FIFO becomes empty. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of RD#, on the last byte, if no edge is present on DACK#). A data underrun may occur if DRQ is not removed in time to prevent an unwanted cycle.

DMA Mode, Transfers from the Host to the FIFO

The 82077AA activates the DRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the DACK# and WR# pins and placing data in the FIFO. DRQ remains active until the FIFO becomes full. DRQ is again set true when the FIFO has <threshold> bytes remaining in the FIFO. The 82077AA will also deactivate the DRQ pin when TC becomes true (qualified by DACK#), indicating that no more data is required. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of WR# of the last byte, if no edge is present on DACK#). A data overrun may occur if DRQ is not removed in time to prevent an unwanted cycle.

Data Transfer Termination

The 82077AA supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer. If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the 82077AA will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the 82077AA, the internal sector count will be complete when 82077AA reads the last byte from its side of the FIFO. There may be delay in the removal of the transfer request signal of up to the time taken for the 82077AA to read the last 16 bytes from the FIFO. The host must tolerate this delay.

Result Phase

The generation of INT determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the 82077AA before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read from the FIFO. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared. This indicates that the 82077AA is ready to accept the next command.

82077AA CHMOS Single-Chip Floppy Disk Controller

SENSE INTERRUPT STATUS

An interrupt signal on INT pin is generated by the 82077AA for one of the following reasons:

1. Upon entering the Result Phase of:
   a.READ DATA Command
   b.READ TRACK Command
   c.READ ID Command
   d.READ DELETED DATA Command
   e.WRITE DATA Command
   f.FORMAT TRACK Command
   g.WRITE DELETED DATA Command
   h.VERIFY Command
2. End of SEEK, RELATIVE SEEK or RECALIBRATE Command.
3. 82077AA requires a data transfer during the execution phase in the non-DMA Mode.

The SENSE INTERRUPT STATUS command resets the interrupt signal and via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt. If a SENSE INTERRUPT STATUS command is issued when no active interrupt condition is present, the status register STO will return a value of 80h (invalid command).

Table 5-7. 82077AA Interrupt Identification

SE	IC	Interrupt Due To
0	11	Polling
1	00	Normal Termination of SEEK or RECALIBRATE command
1	01	Abnormal Termination of SEEK or RECALIBRATE command

The SEEK, RELATIVE SEEK and the RECALIBRATE commands have no result phase. SENSE INTERRUPT STATUS command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in STO will always return a "0". If a SENSE INTERRUPT STATUS is not issued, the drive, will continue to be BUSY and may effect the operation of the next command.

Compatibility

The 82077AA was designed with software compatibility in mind. It is a fully backwards compatible solution with the older generation 8272A and NEC765A/B disk controllers. The 82077AA also implements on-board registers for compatibility with the Personal System/2s as well as PC/AT and PC/XT floppy disk controller subsystems. Upon a hardware reset of the 82077AA, all registers, functions and enhancements default to a PS/2, PC/AT, or PS/2 Model 30 compatible operating mode depending on how the IDENT and MFM pins are sampled during Hardware Reset.

Register Set Compatibility

The register set contained within the 82077AA is a culmination of hardware registers based on the architectural growth of the IBM personal computer line. Table 5-8 indicates the registers required for compatibility based on the type of computer.

Table 5-8. 82077AA Register Support

82077AA Register	8272A	82072	PC/XT	PC/AT	PS/2	MOD 30
SRA					X	X
SRB					X	X
DOR			X	X	X	X
MSR	X	X	X	X	X	X
DSR		X				
Data (FIFO)	X	X	X	X	X	X
DIR				X	X	X
CCR		X		X	X	X

PS/2 vs. AT vs. Model 30 Mode

To maintain compatibility between PS/2, PC/AT, and Model 30 environments the IDENT and MFM pins are provided. The 82077AA is placed into the proper mode of operations upon Hardware RESET with the appropriate settings of the IDENT and MFM pins. The proper settings of the IDENT and MFM pins are described in IDENT's pin description. Differences between the three modes are described in the following sections.

PC/AT Mode

IDENT strapped high causes the polarity of DENSEL to be active high for high (500 Kbps/1 Mbps) data rates (typically used for 5.25-inch drives). This polarity of DENSEL assumes INVERT# to be low.

If the DMAGATE bit is written to a "0" in the Digital Output Register (DOR), DRQ and INT will tristate. If DMAGATE is written to a "1", then DRQ and INT will be driven appropriately by the 82077AA.

TC is an active high input signal that is internally qualified by DACK# being active low.

82077AA PC/AT Solution

The 82077AA integrates the entire PC/AT controller design with the exception of the address decode on a single chip. The chip select for the 82077AA is generated by a 16L8 PAL that is programmed to decode addresses 03F0h thru 03F7h when AEN(Address Enable)is low. An alternative address decode solution could be provided by using a 74LS133 13-input NAND gate and 74LS04 invertor to decode A3-A14 and AEN. Although the PC/AT allows for a 64K I/O address space, decoding down to a 32K I/O address space is sufficient with the existing base of add-in cards.

A direct connection between the disk interface and the 82077AA is provided by on-chip output buffers with a 40 mA sink capability. Open collector outputs from the disk drive are terminated at the disk controller with a 150 Ω resistor pack. The 82077AA disk interface inputs contain a schmitt trigger input structure for higher noise immunity. The host interface is a similar direct connection with 12 mA sink capabilities on DB0-DB7, INT and DRQ.

An I/O address map of the complete register set for the PC/AT floppy disk controller is shown in Table 5-9.

Table 5-9. 82077AA I/O Address Map for the PC/AT

I/O Address	Access Type	Description
3F0h	—	Unused
3F1h	—	Unused
3F2h	Write	Digital Output Register
3F3h	—	Unused
3F4h	Read	Main Status Register
3F5h	Read/Write	Data Register
3F6h	—	Unused
3F7h	Write	Data Rate Select Register
3F7h	Read	Digital Input Register

Table 5-10 indicates the drive and media types the PC/AT disk controller can support.

Table 5-10. 82077AA Standard PC/AT Drives and Media Formats

Capacity	Drive Speed	Data Rate	Sectors	Cylinders
360 KB	300 RPM	250 Kbps	9	40
360 KB*	360 RPM	300 Kbps	9	40
1.2 MB	360 RPM	500 Kbps	15	80

*360 Kbyte diskette in a 1.2 Mbyte drive

3½-inch Drive Interfacing

The 82077AA is designed to interface to both 3½-inch and 5¼-inch disk drives. This is facilitated by the 82077AA by orienting IDENT to get the proper polarity of DENSEL for the disk drive being used. Typically DENSEL is active high for high (500 Kbps/1 Mbps) data rates on 5¼-inch drives. And DENSEL is typically active low for high data rates on 3½-inch drives.

3½-inch Drives under the AT Mode

When interfacing the 82077AA floppy disk controller with a 3½-inch disk drive in a PC/AT application, it is possible that two design changes will need to be implemented for the design discussed in "82077AA PC/AT Solution" above. Most 3½-inch disk drive incorporate a totem pole interface structure as opposed to open collector.

Outputs of the disk drive will drive both high or low voltage levels when the drive is selected, and float only when the drive has been deselected. These totem pole outputs generally can only sink or source 4 mA of current. As a result, it is recommended to replace the 150 Ω termination resistor pack with a 4.7 KΩ package to pull floating signals inactive. Some other 3½-inch drives do have an open collector interface, but have limited sink capability. In these cases, the drive manufacturer manuals usually suggest a 1 KΩ termination.

A second possible change required under "AT mode" operation involves high capacity 3½-inch disk drives that utilize a density select signal to switch between media recorded at a 250 Kbps and 500 Kbps data rate. The polarity of this signal is typically inverted for 3½-inch drives versus 5¼-inch drives. Thus, an invertor can be added between the DENSEL output of the 82077AA and the disk drive interface connector when using 3½-inch drives.

But drives that do not support both data rates or drives with an automatic density detection feature via an optical sensor do not require the use of the DENSEL signal.

Another method is to change the polarity of IDENT with a drive select signal. ORing RESET with the drive select signal (DS0-3) used for the 3½-inch disk drive will produce the proper polarity for DENSEL (assuming INVERT# is low).

For the complete data sheet on 82077AA, please refer to Intel's *Peripheral Components* data book, order number: 296467-002.

WD90C20 VGA Controller

Description and Application

The WD90C20 is a VGA display controller that has been optimized for applications that require flat panel display support. It is an extension of the WD90C00 and as such supports all of the WD90C00's features and modes when driving a standard CRT. The WD90C20's highly integrated design includes a complete Micro Channel or AT-compatible bus interface, as well as an on-chip PS/2 compatible RAMDAC with integral monitor detection logic. The controller's 1.25 micron CMOS construction and power-management features significantly reduce the power required for the display subsystem.

Flat panel displays supported include all 640 by 480 monochrome and color liquid crystal displays (LCD), as well as Plasma displays.

Features of the WD90C20 VGA controller include:

- On-chip Micro Channel interface
- On-chip 8- or 16-bit AT bus interface
- Directly drives CRT, Plasma and monochrome and color LCD displays
- On-chip frame rate modulation logic
- Supports all functions of WD90C00 VGA chip in CRT mode
- 32-, 16-, or 8-shade gray scale mapping
- Software-selectable vertical screen centering
- On-chip PS/2-compatible RAMDAC
- On-chip monitor detection logic
- 45 MHz maximum video clock
- Flexible power management features
- VCC may be removed in powered system
- 256 color support for TFT and DSTN color LCDs

Theory of Operation

The WD90C20 contains six major functional modules. In addition to the CRT controller, there is a sequencer, a graphics controller, an attribute controller, a flat panel interface, and a RAMDAC. The WD90C20 handles all display buffer management functions, including display refresh cycles, memory refresh cycles, and the arbitration and sequencing of host access cycles.

Sequencer

The sequencer provides the display memory control signals and timing. It also provides the synchronization between the CRT controller and the attribute controller. The sequencer controls the arbitration between the CPU cycle and the CRT cycle, or the CPU cycle and the memory refresh cycle.

Graphics Controller

The graphics controller manages data flow between video memory and the attribute controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the sequencer.

Attribute Controller

The attribute controller modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, scrolling, reverse video (as well as background or foreground video) in VGA and enhanced VGA BIOS modes.

Flat Panel Adapter

The flat panel adapter section includes color-to-gray scale mapping, RAM mapping, shading control, and panel interface logic.

RAMDAC

The WD90C20's on-board RAMDAC is a low power, PS/2-compatible device with special power down modes and PS/2 monitor detection logic.

The RAMDAC's 256 by 18 color look-up table has triple 6-bit D/A converters, a pixel mask register, and composite blank generation on the three channels. Options supported include a programmable pedestal (0 or 7.5 IRE) and the use of an external voltage reference. Without external buffering the RAMDAC will generate RS-343A-compatible video signals into a singly terminated 75 Ω load. Integral and differential linearity errors are a maximum of ± ¼ LSB.

WD90C20 Interfaces

The WD90C20 has five main system interfaces: the CPU, a display memory, a RAMDAC/CRT, a clock, and a flat panel display. In most implementations, these interfaces eliminate the need for glue logic.

CPU Interface

The WD90C20 host interface supports both the AT and Micro Channel buses with both eight and sixteen bit data path widths. The WD90C20 may also be directly connected to the bus if drive requirements permit. The bus mode is determined by the status of the configuration register bit, CNF(2), which is loaded by the de-assertion of reset. The value that is loaded reflects the status of one of the memory data pins at reset.

I/O transfers to and from the device are eight bits wide, and display memory transfers are eight or sixteen bits wide, depending on the video mode selected. Because of their architecture, EGA type planar modes are restricted to eight bit display data transfers. Text and 256 color extended modes allow 16 bit transfers on a 16 bit bus.

The controller generates wait states as required during display memory accesses. Wait states are not generated for I/O or video BIOS ROM accesses. Special I/O ports, such as 46E8h (when in AT bus mode) for setup, and 102h for VGA enable, are internally implemented.

Display Memory Interface

The WD90C20 generates all signals and memory timing required to operate the display memory. It directly controls three display memory sizes, 256K, 512K, and one megabyte, as shown in Table 5-11.

Table 5-11. WD90C20 Memory Sizes

Memory Size	No. and Type of DRAM Required
256 KB	8 64K x 4 DRAMs, or 2 64K x 16 DRAMS
512 KB	16 64K x 4 DRAMs or 4 64K x 16 DRAMs
1 MB	8 64K x 16 DRAMs or 8 256K x 4 DRAMs

Page mode memories are required for all configurations. With a 36 MHz memory clock (MCLK), 120 ns devices may be used. If 256 color CRT modes are to be supported, 100 ns DRAMs and a 45 MHz MCLK are required. The WD90C20 includes special offset registers that allow the host to address up to 1 MB of display memory.

CRT/RAMDAC Interface

In addition to its internal RAMDAC, the WD90C20 allows the use of an external RAMDAC. This is helpful in specialized applications where a 24-bit wide color lookup table or pixel demultiplexing (to obtain higher video rates) is required. The external RAMDAC interface will support any Bt471/478/476 compatible device.

Clock Interface

The WD90C20 has four clock input signal pins. Three of these (VCLKO, VCLK1, and VCLK2) are normally connected to oscillators. VCKL1 and VCLK2 may be configured to control an external clock multiplexor or clock generator, such as the WD90C61. In this configuration, VCLK0 becomes the clock input while VCLK1 and VCLK2 become outputs used to drive the multiplexor select inputs.

The memory clock input, MCLK, is used by the internal logic to generate all memory timing and may be up to 36 MHz for 120 ns DRAMs or 45 MHz for 100 ns DRAMs.

Flat Panel Interface

The WD90C20 is designed to interface with 640 by 480 LCD or Plasma panels. The flat panel interface lines change function to support the specific panel type chosen. Table 5-12 summarizes their use for each mode of operation.

When in LCD mode with frame rate modulation selected, the controller supplies 8 pixels per shift clock (four for the upper panel and four for the lower). If pulse width modulation is selected, the controller provides two pixels per shift clock (one four bit pixel for the upper screen and one four bit pixel for the lower screen).

When in Plasma mode, pulse width modulation is used to provide shading, while the controller supplies one pixel (four bits per pixel) per clock.

When in color STN LCD mode, the controller supplies 2 pixels per shift clock and uses hardware dithering. Each pixel (three bits, one each for R, G, and B), with dithering, provides 16 colors. The user can select any 16 out of 26 colors by programming a 32 x 5 mapping RAM.

Table 5-12. Display Interface Output Functions

LCD	PLASMA	CRT
UD (3:0)	VD (3:0)	P (7:4)
LD (3:0)	Reserved	P (3:0)
FR	Reserved	BLANK
FP	VS	VSYNC
LP	HS	HSYNC
XSCLK	XSCLK	Reserved
WGTCLK	ENABLE	Reserved
Reserved	Reserved	PCLK

Table 5-13. LCD Data Bit Assignments

Monochrome LCD	Color LCD
UD (3)	B1
UD (2)	G1
UD (1)	R1
UD (0)	Border Information
LD (3)	B2
LD (2)	G2
LD (1)	R2
LD (0)	Reserved

Power-Up Configuration

An internal eight-bit configuration register, CNF, controls the behavior of the major interfaces. Its bits are loaded with the inverted state of memory data lines 0 through 7 at the time RESET is deasserted. Pull-up or pull-down resistors on the MD lines are used to set the configuration.

Flat Panel Support Considerations

Supporting VGA compatible graphics on flat panel displays involves several non-trivial issues, including:

- Display timing differences
- Screen size mapping
- Color-to-gray scale mapping
- Shading mechanics
- Split screen refresh

The following paragraphs address each of these issues.

Display Timing Differences

Typically, flat panel displays have different timing requirements from a CRT. To overcome this problem, the WD90C20 provides a set of hidden display timing registers, which are read/write protected in locked mode.

Screen-Size Mapping

Unlike those of a CRT, the pixels on a flat panel display are real, discrete entities of a fixed size. This can result in problems when different display modes are mapped onto a single panel. The WD90C20 has been designed to support VGA and various backward compatible display modes on a 640 by 480 dot flat panel and it provides integral hardware support to deal with screen size incompatibilities.

In case of backward compatible display modes, such as EGA, which has a maximum resolution of 640 by 350, the vertical resolution of the mode is less than the number of dots of vertical resolution of the panel. This results in an active display area that is smaller than that of the panel and shifted up on the display. There are two ways to handle such situations, both of which are supported by the WD90C20.

The simplest approach is to keep the vertical resolution of the display mode constant but center the active display area vertically on the panel. In the case of an EGA 350 line mode being displayed on a 480 line panel, this would involve shifting the active display area down 65 lines (that is, 480 minus 350, the quantity divided by two).

If the goal is to have the active display area fill the panel in all modes, then the active display area can be expanded by double scanning a portion of the active scan lines. Previously available controllers simply double scan lines at regular intervals, every third line in the case of EGA 350 line modes.

Future revisions of the WD90C20 will use an advanced proprietary algorithm that automatically expands to fill all 480 lines. This algorithm can be used to support better "screen scrolling" when in 350 line modes.

Under certain display conditions, any expansion scheme can result in undesirable aliasing effects of the displayed data. For this reason the WD90C20 allows the system designer flexibility to choose between vertical expansion or centering as appropriate.

Horizontal resolution issues involve 720 dot modes such as VGA text and Hercules graphics. In VGA test mode, the 9th dot in each character box is dropped. The net effect is a slight compression in the spacing between characters. Alternatively, a different font may be loaded, although a nonstandard font size may not be fully compatible.

Color-to-Gray-Scale Mapping

The VGA standard defines how colors are mapped to 64 gray scale values on monochrome monitors. The mapping is based on the following RGB weighting equation:

$$I = .30R + .59G + .11B$$

Unfortunately, many of the currently available panels support at most sixteen shades and some support two. In order to provide faithful support of all of the standard VGA modes on a flat panel, the WD90C20 provides a range of features to map colors to intensities and control panel shading. Foremost among these is sophisticated logic that converts gray scale values into dithering patterns. Additionally, the device allows software modification of the weighting values used in the gray scale mapping equation.

Shading Mechanics

The WD90C20 supports shading via either frame rate or pulse width modulation. Pulse width modulation is handled via the display panel. The controller transfers 2, 3, or 4 bits per pixel to the driver logic on the panel, along with a high speed clock signal used to sequence the shading logic. Frame rate modulation, on the other hand, must be implemented in the display controller. The WD90C20 provides support for 2, 4, 8, 16, or 32 shade frame rate modulation with its integrated dithering controller. Any combination of dithering patterns can be selected via the dithering controller's mapping RAM. This design allows the WD90C20 to provide flicker-free frame rate modulation with frame rates as low as 70 Hz.

Split Screen Refresh

The WD90C20 provides complete support for panels that are split into upper and lower panels requiring simultaneous refresh. This type of refresh is typically used by non-active matrix LCDs and plasma panels.

WD90C61 VGA Dual Clock Generator

Introduction

The Western Digital Imaging WD90C61 is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, the other is the video dot clock.

The WD90C61 Video Graphics Array clock generator is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with every Western Digital Imaging Video Graphics Array device to optimize video subsystem performance.

The video dot clock output may be one of six internally generated frequencies or one of two external inputs. The selection of the video dot clock frequency is done through four inputs: VSELO, VSEL1, VGA/TTL, and FCLKSEL. The video clock selection is latched by the SELEN signal (see Table 5-14).

The inputs and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers. When a Western Digital Imaging controller is used with a WD90C61, two of the VGA's video clock inputs become outputs and directly drive the SELEN and VGA/TTL inputs.

The WD90C61 generates the VCLK output as shown in Table 5-14. The VSELO and VSEL1 inputs are latched with SELEN. VGA/TTL is an additional select input that selects frequencies for VGA modes when left high and frequencies for TTL modes when pulled low. Select input FCLKSEL overrides internal clock generation and passes through the FCLKIN clock input.

The MCLK output is generated as shown in Table 5-15. The various VCLK and MCLK frequencies are achieved by multiplying the 14.318 MHz input frequency by a factor of N/32 (e.g., 44.74 is obtained with N = 100).

The VCLKEN and MCLKEN inputs can tri-state the VCLK and MCLK outputs to facilitate board level testing. External filter components are attached to the MCAP and VCAP pins for the internal phase lock loops.

Features of the WD90C61 Dual Clock Generator include:

- Clock generator for the IBM compatible Western Digital Imaging Video Graphics Array (VGA) chips.
- Generates six video clock frequencies (25.057, 28.189, 36.242, 16.108, 32.216 and 44.744 MHz) derived from a 14.318 MHz system clock frequency.
- On-chip generation of four (36.242, 41.612, 37.586 and 44.744 MHz) memory clock frequencies.
- Video clock is selectable among the six internally generated clocks and two external clocks.
- CMOS technology.
- 20-pin PLCC package.

Table 5-14. VCLK Selection

VCLKEN	FCLKSEL	VGA/TTL	VSELO	VSEL1	SELEN+ *	VCLK FREQUENCY
Open	1 or Open	1 or Open	0	0	↑	25.057 MHz
Open	1 or Open	1 or Open	0	1	↑	28.189 MHz
Open	1 or Open	1 or Open	1	0	↑	EXTCLK pass-through
Open	1 or Open	1 or Open	1	1	↑	36.242 MHz
Open	1 or Open	0	0	0	↑	14.318 MHz
Open	1 or Open	0	0	1	↑	16.108 MHz
Open	1 or Open	0	1	0	↑	32.216 MHz
Open	1 or Open	0	1	1	X	44.744 MHz
Open	0	X	X	X	X	FCLKIN pass-through

* Rising edge for SELEN (↑)

Table 5-15. MCLK Selection

MCLKEN	MSELO	MSEL1	MCLK FREQUENCY
Open	1 or Open	1 or Open	44.744 MHz
Open	1 or Open	0	37.585 MHz
Open	0	1 or Open	36.242 MHz
Open	0	0	41.612 MHz
0	X	X	Disabled

WD90C61 Interface

The WD90C61 has three system interfaces: System Bus, Feature Connector and VGA Controller, as well as analog filters and other user programmed inputs. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs VCLK1 and VCLK2 to outputs. These outputs are used to select the required video clock frequency.

System Bus Inputs

The system bus inputs are listed below:

CLK1
VSELO
VSEL1

The WD90C61 uses 14 MHz system bus clock as a reference to generate all its frequencies for both video and memory clocks. Address lines D2 and D3 are also commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

VGA Controller Inputs

The VGA controller inputs are listed below:

VGA/TTL
SELEN

The WD90C61 is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, and VGA/TTL. The signal VGA/TTL may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs VGA/TTL, VSEL0, and SVEL1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to 3C2h.

VGA Controller Outputs

The VGA controller outputs are listed below:

MCLK
VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

Feature Connector Inputs

The feature connector inputs are listed below:

FCLKIN
FCLKSEL

There are two inputs from the feature connector: FCLKIN and FCLKSEL. FCLKIN may be used as an alternate video clock. FCLKIN becomes the selected video clock if FCLKSEL goes low.

Analog Filters

The analog filters are listed below:

MCAP
VCAP

These connections are for the analog filters. The component values of the filters are critical. Care must be taken to ensure proper values over the entire operating range desired for the final product. The capacitor tolerances are ± 20%. The resistor tolerance is 2%.

User Definable Inputs

The user definable inputs are listed below:

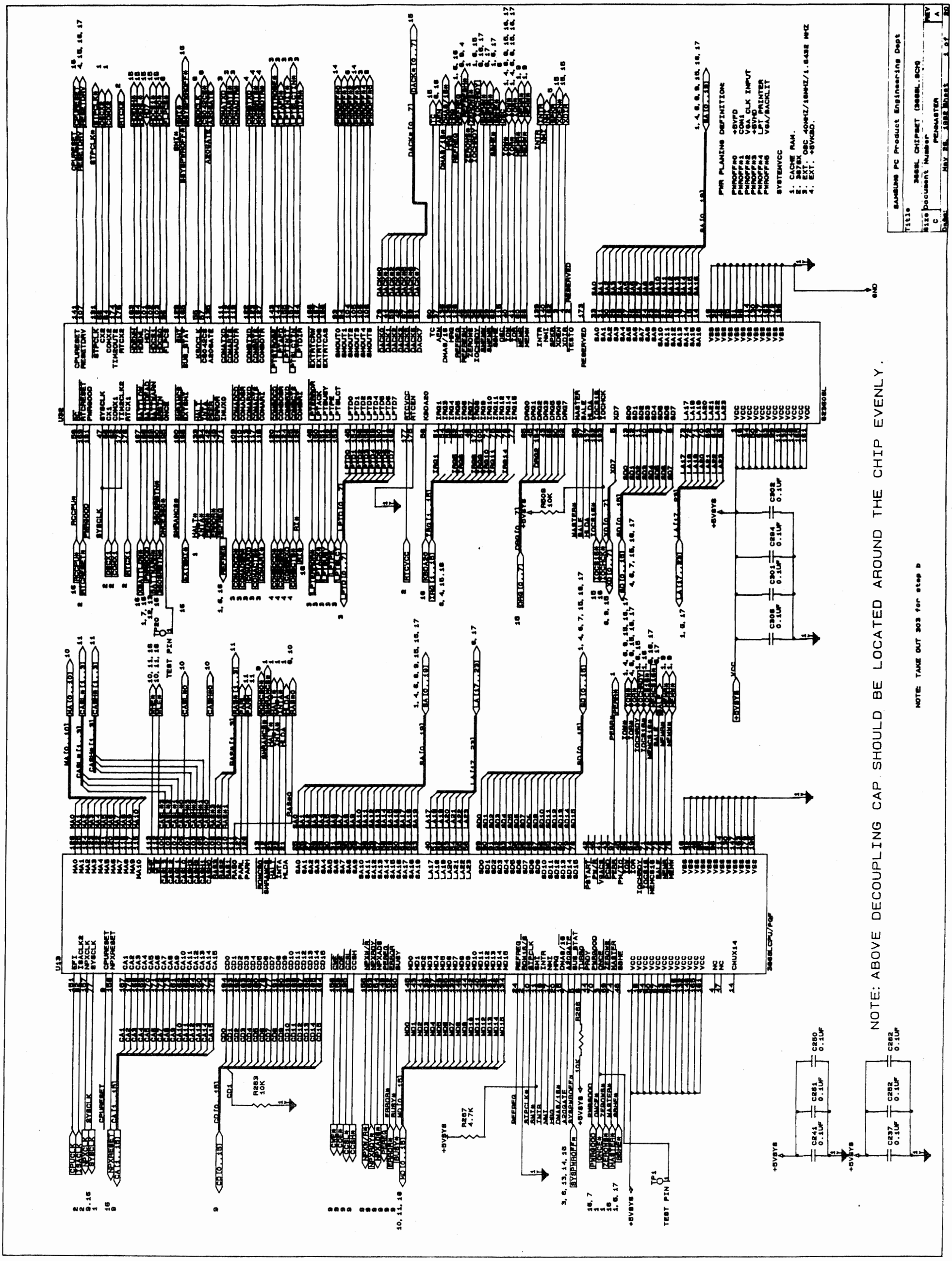
EXTCLK
VCLKEN
MCLKEN
MSEL0
MSEL1

EXTCLK is an additional input that may be routed to the VCLKO output. This additional input is useful for supporting modes that require frequencies not provided by the WD90C61. VCLKEN and MCLKEN are the output enable signals for VCLK and MCLK.

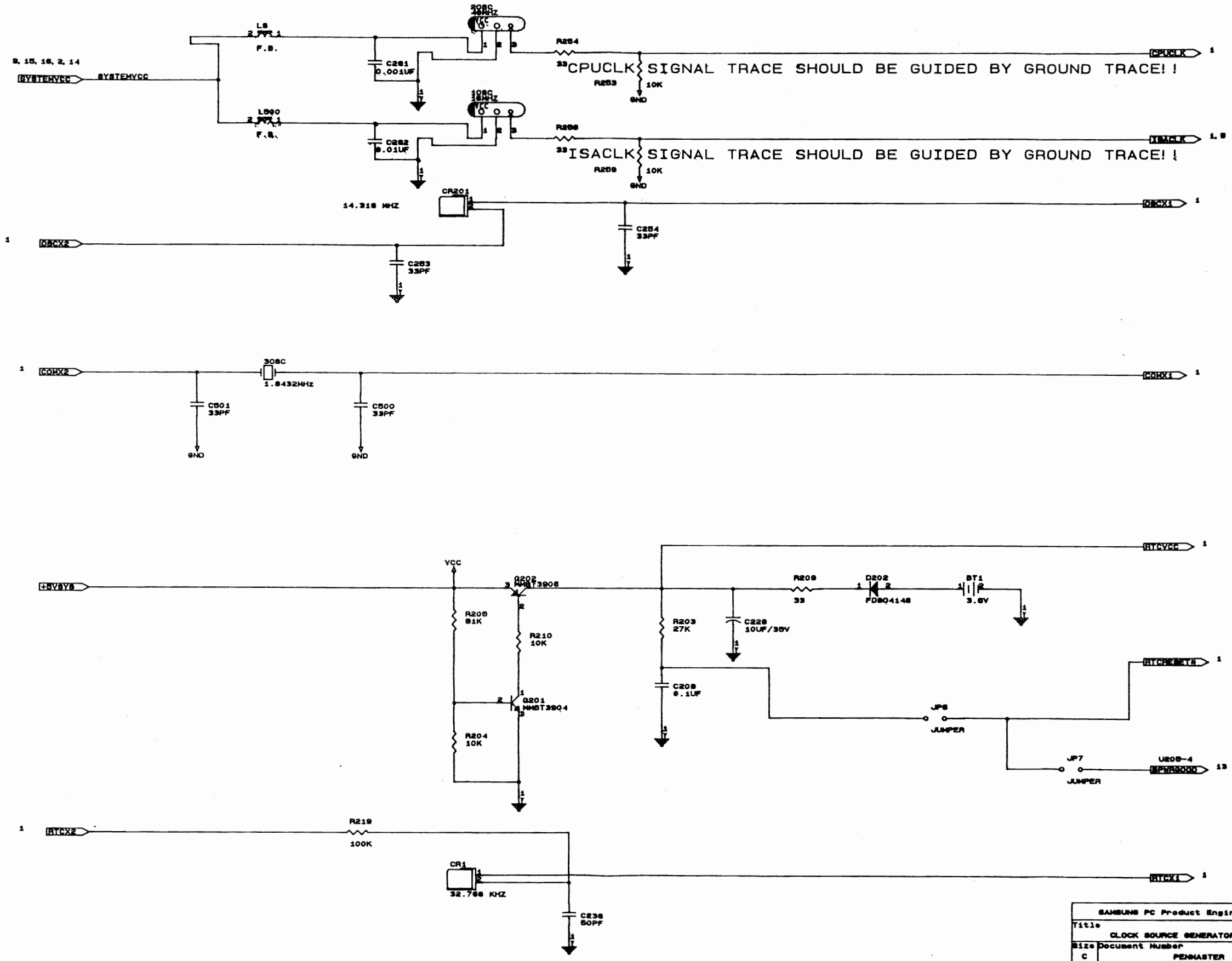
MSEL0 and MSEL1 are the memory clock (MCLK) select lines. Table 5-15 shows how MCLK frequencies are selected. All signals in this group have internal pullup resistors.

Appendix A

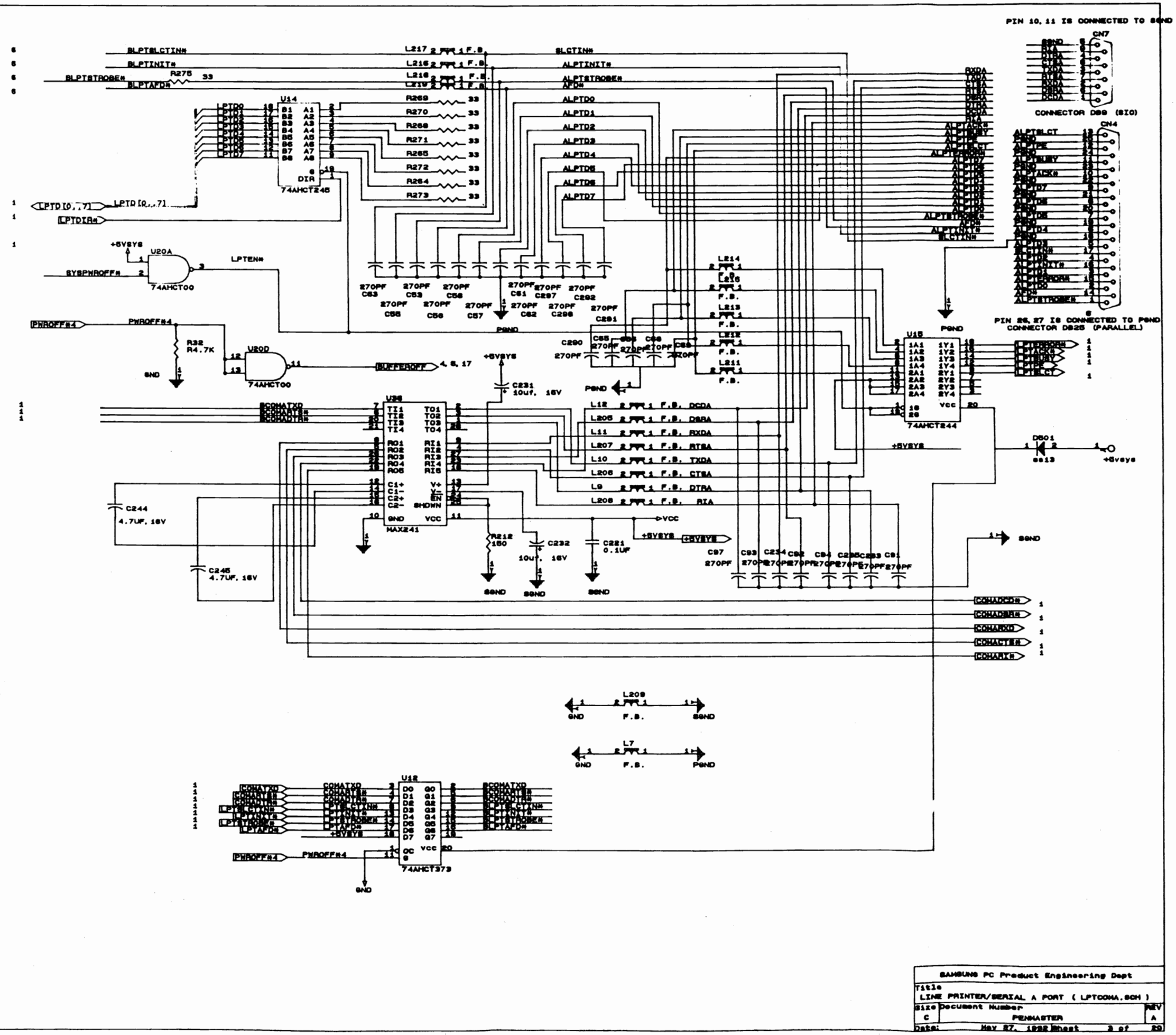
Schematic Diagrams


SAMSUNG PC Product Engineering Dept
Title
386SL CHIPSET (386SL.SCH)
Size C
Document Number
PENMASTER
REV A
Date: May 28, 1992 Sheet 1 of 20
PWR PLANING DEFINITION:
PHROFFM0 +5VFD
PHROFFM1 COM1
PHROFFM2 +5V CLK INPUT
PHROFFM3 +5VMOD PRINTER
PHROFFM4 LPT/PRINTER
PHROFFM5 VGA/BACKLIT
SYSTEMVCC
1. CACHE RAM.
2. 386SX
3. EXT. OSC 40MHZ/16MHZ/1.8432 MHZ
4. EXT. +5VCORD.
NOTE: TAKE OUT 303 for step b
NOTE: ABOVE DECOUPLING CAP SHOULD BE LOCATED AROUND THE CHIP EVENLY.

NOTE: ALL OSC/XTAL SHOULD BE PLACED TO CHIP AS CLOSE AS POSSIBLE.

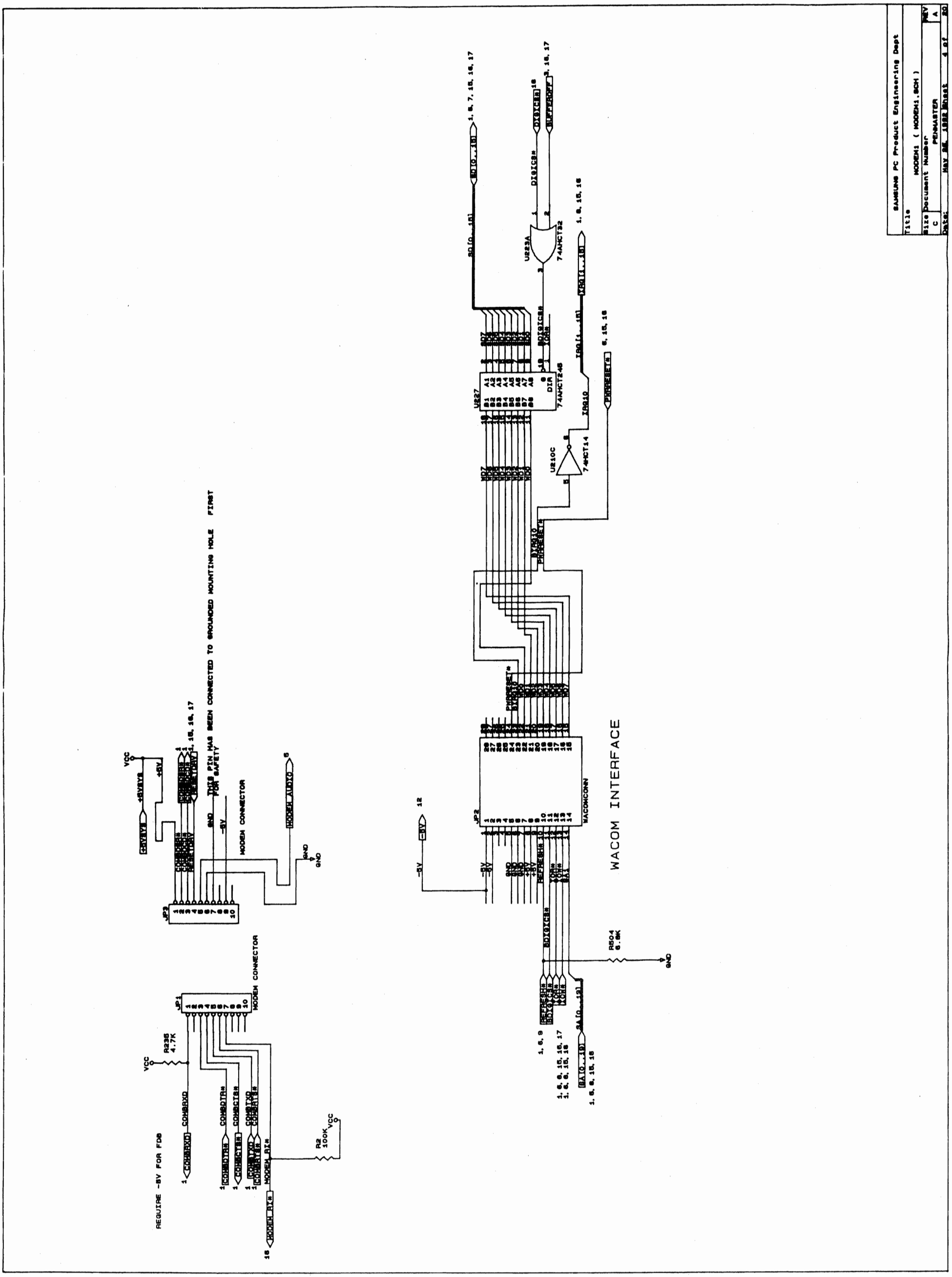


SAMSUNG PC Product Engineering Dept		
Title: CLOCK SOURCE GENERATOR (CLK.SCH)		
Size: C	Document Number: PENMASTER	REV: A
Date: May 27, 1998	Sheet 2 of 20	



Pen Computer Service Manual A-5

SAMSUNG PC Product Engineering Dept			
Title: LINE PRINTER/SERIAL A PORT (LPTCOMA.SCH)			
Size: C	Document Number: PENMASTER		REV: A
Date: May 27, 1992	Sheet 3 of 20		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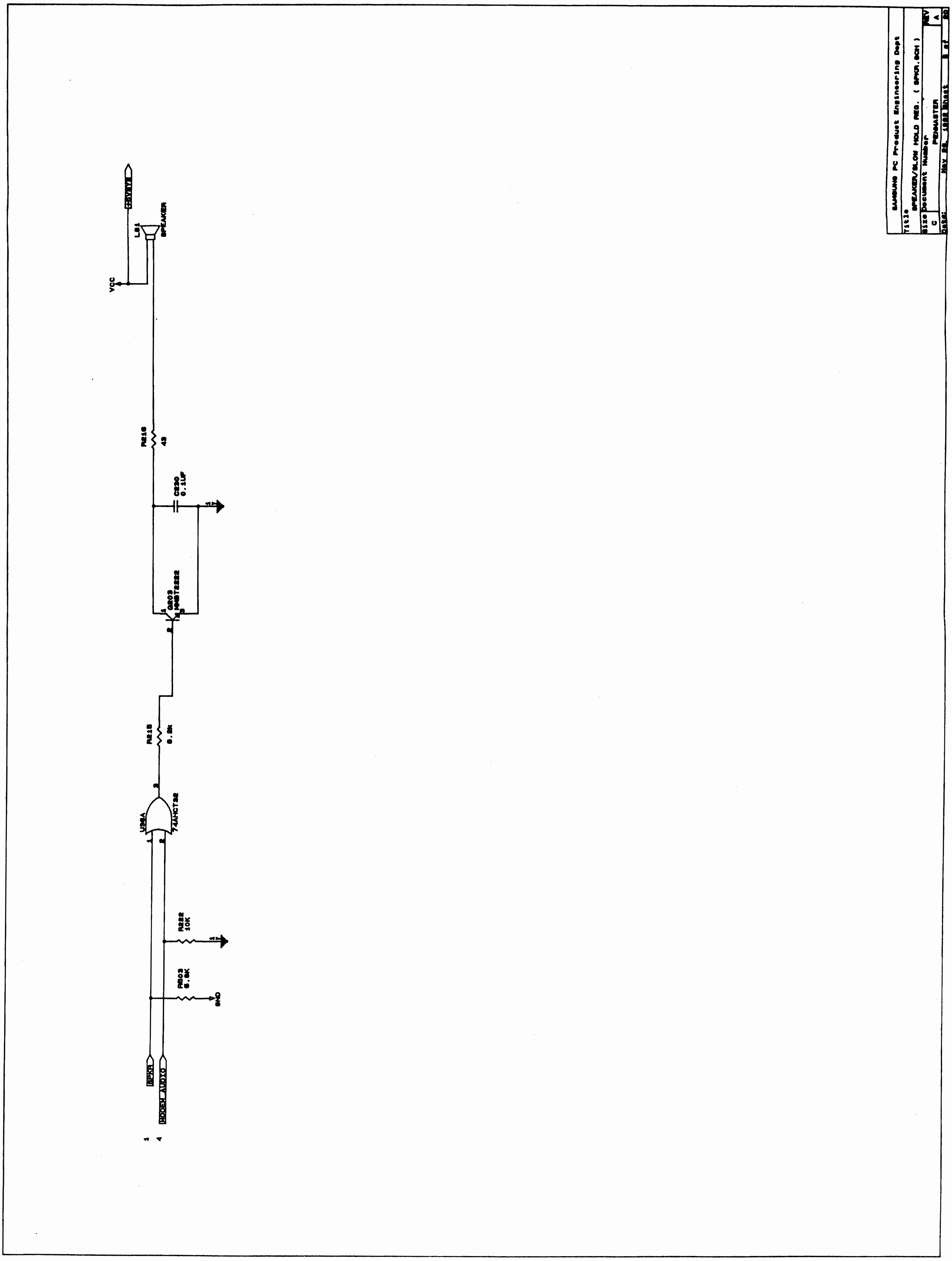
Title
MODEM (MODEM1.SCH)
Size C
Document Number
PENMASTER
REV A
Date: May 06, 1998 Sheet 4 of 20
WACOM INTERFACE
MODEM CONNECTOR
MODEM AUDIO
THIS PIN HAS BEEN CONNECTED TO GROUNDED MOUNTING HOLE FIRST FOR SAFETY
REQUIRE -8V FOR FDB
74AHCT245
74AHCT32
74HCT14
MACOMCONN
R235 4.7K
R2 100K
R504 6.8K


SAMSUNG PC Product Engineering Dept
Title
SPEAKER/SLOW HOLD REG. (SPKR.SCH)
Size
C
Document Number
PENMASTER
REV
A
Date:
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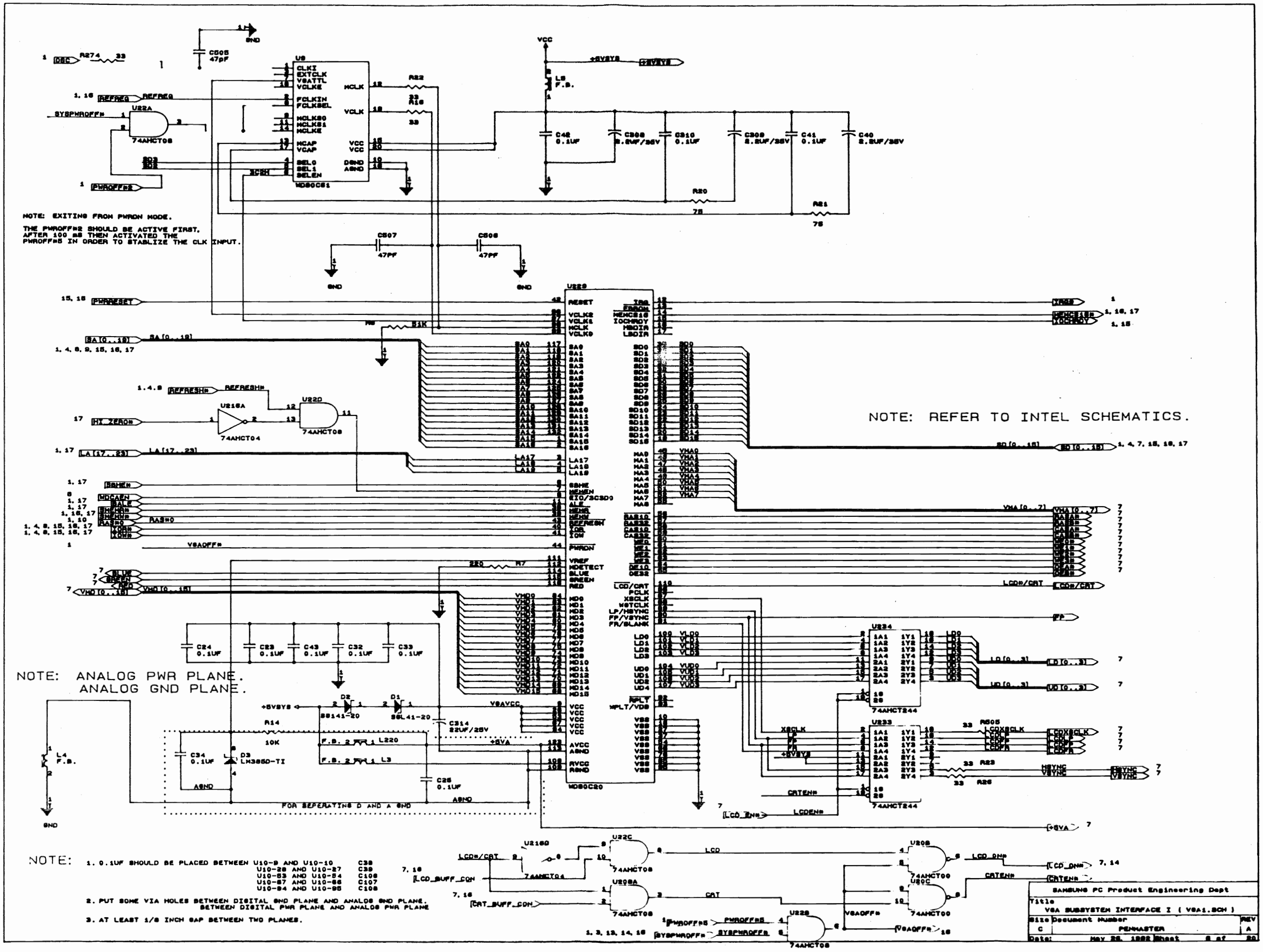
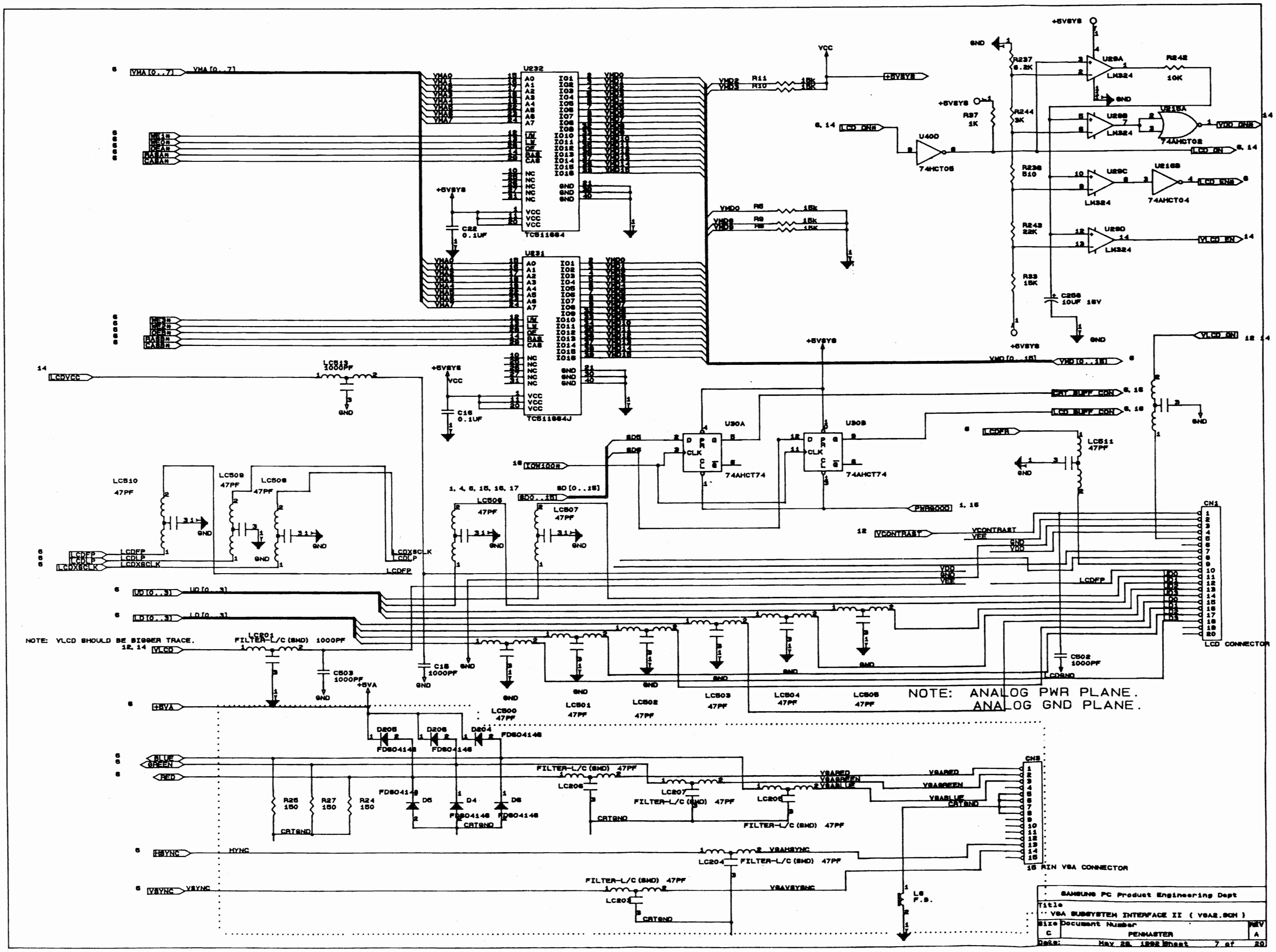
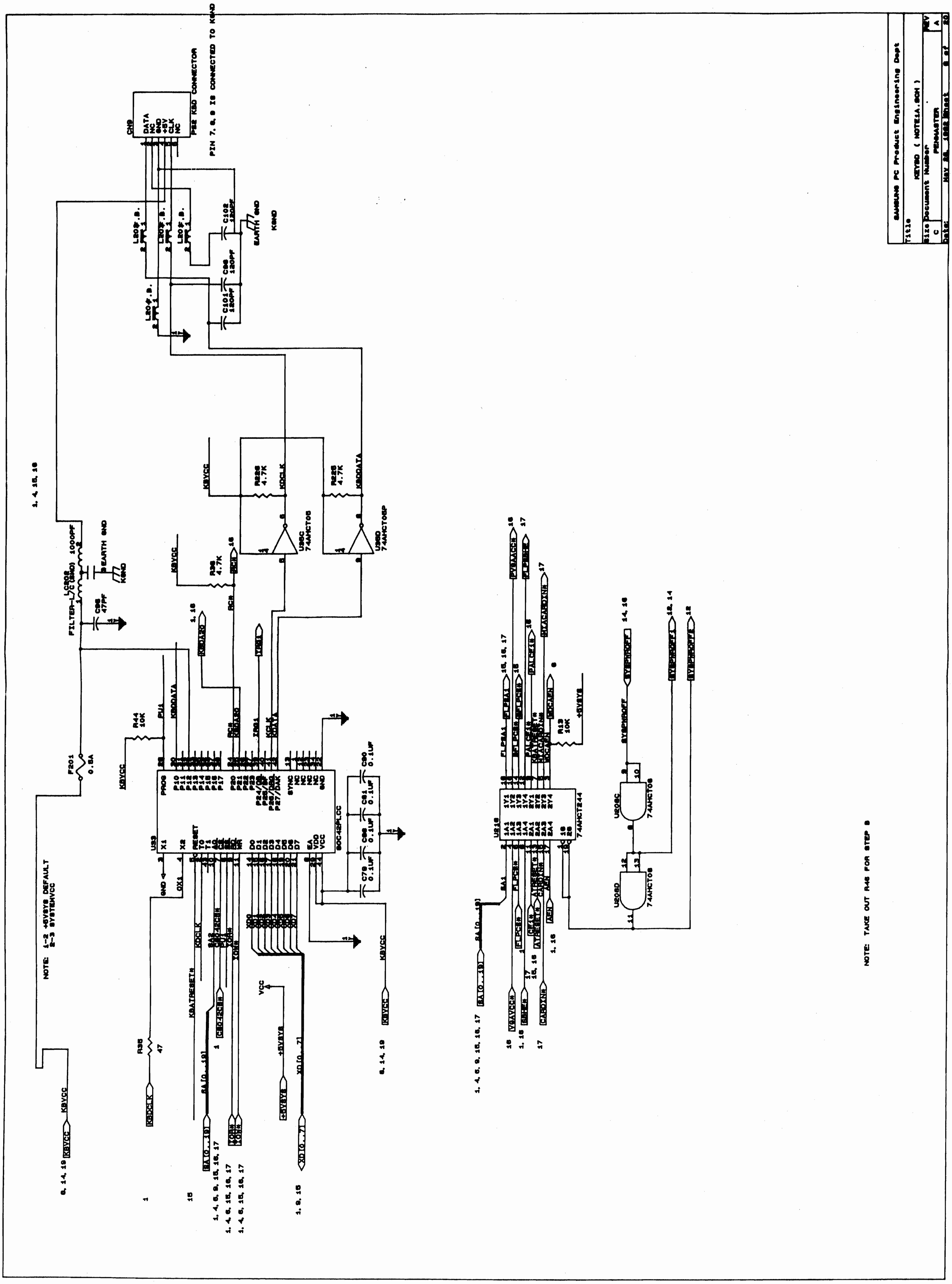
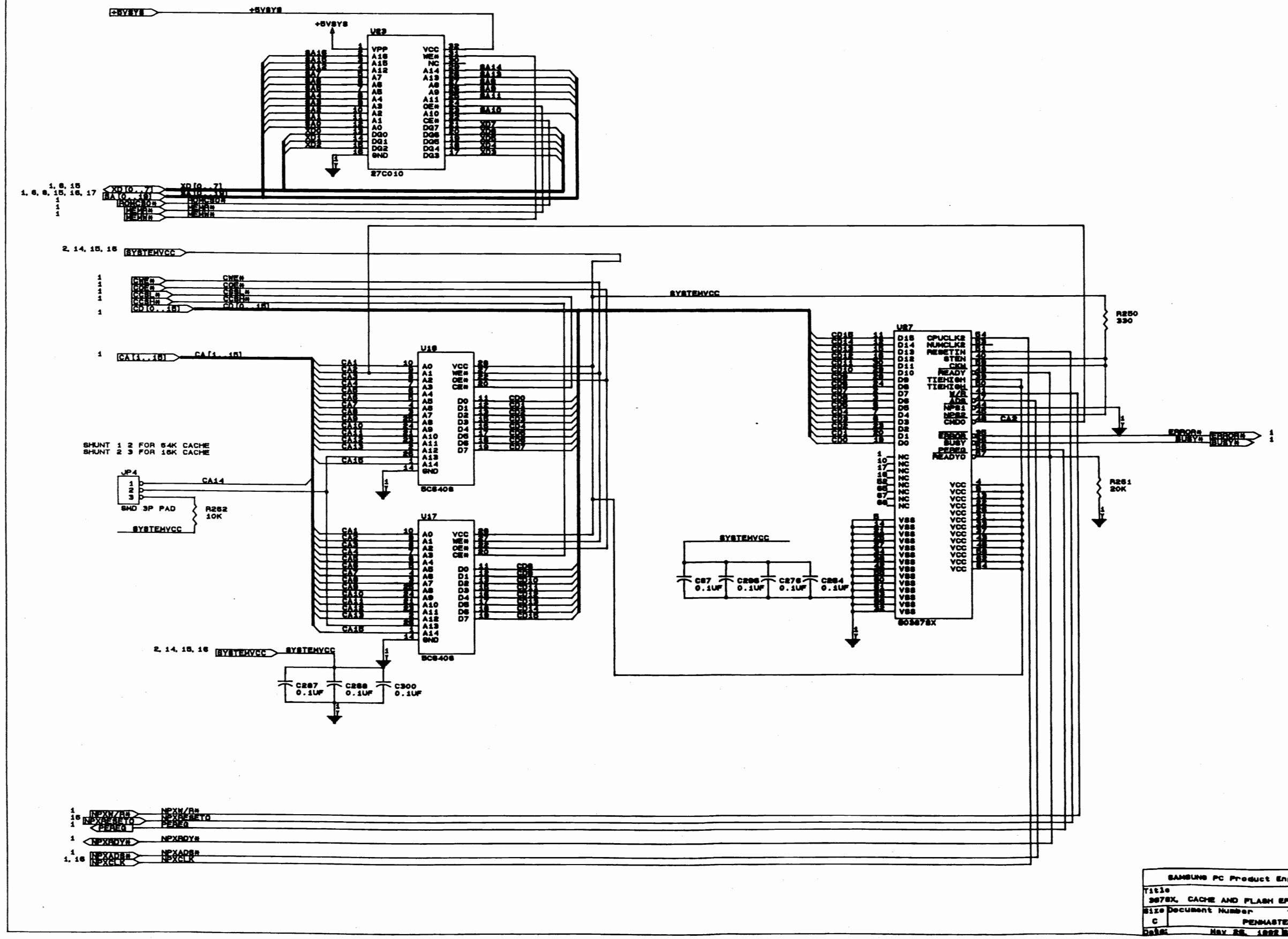
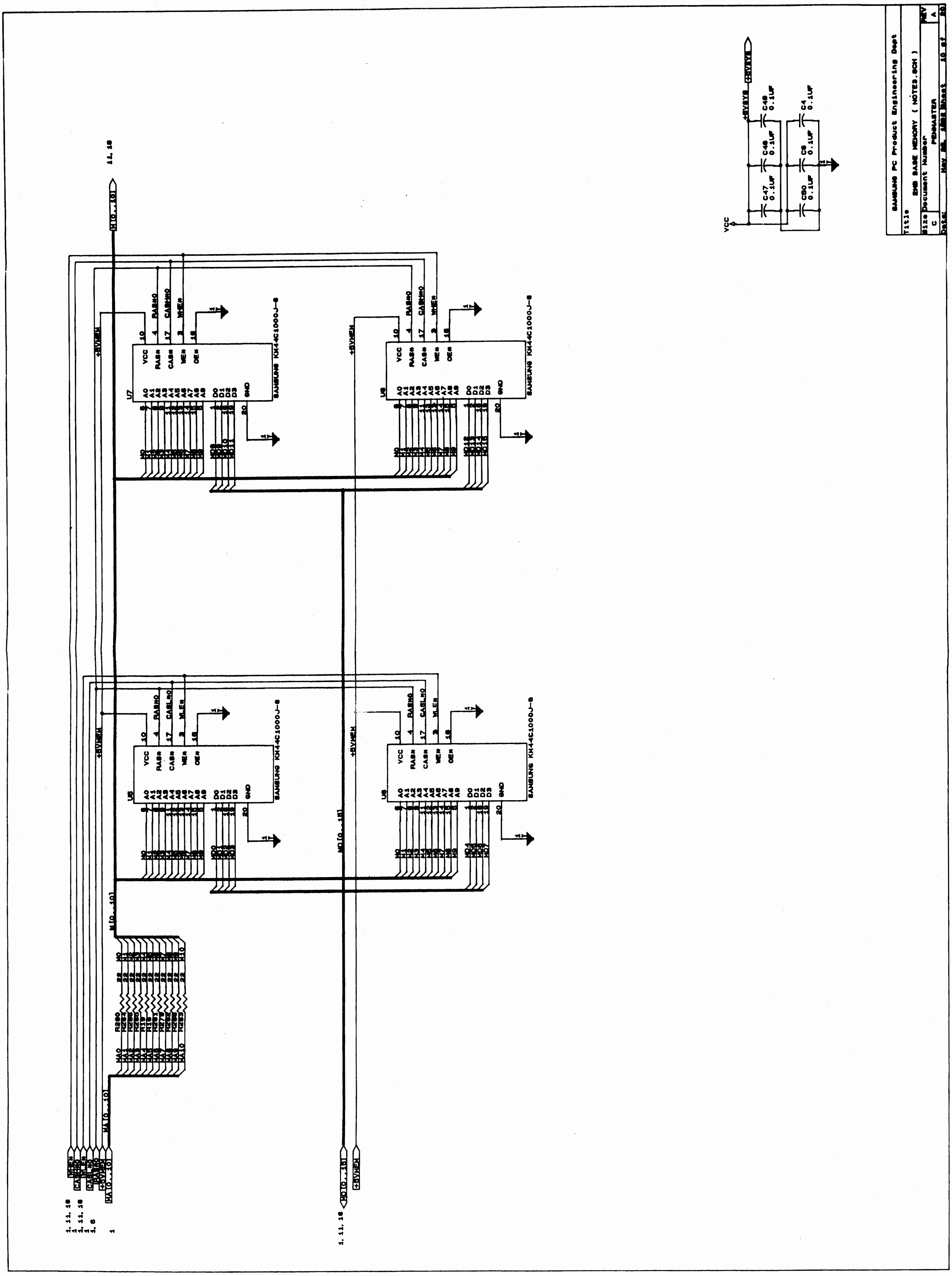
VCC
LS1
SPEAKER
R216
43
C830
0.1UF
Q203
R215
U38A
74AHCT32
R222
10K
GND
SPKR
MODEM AUDIO

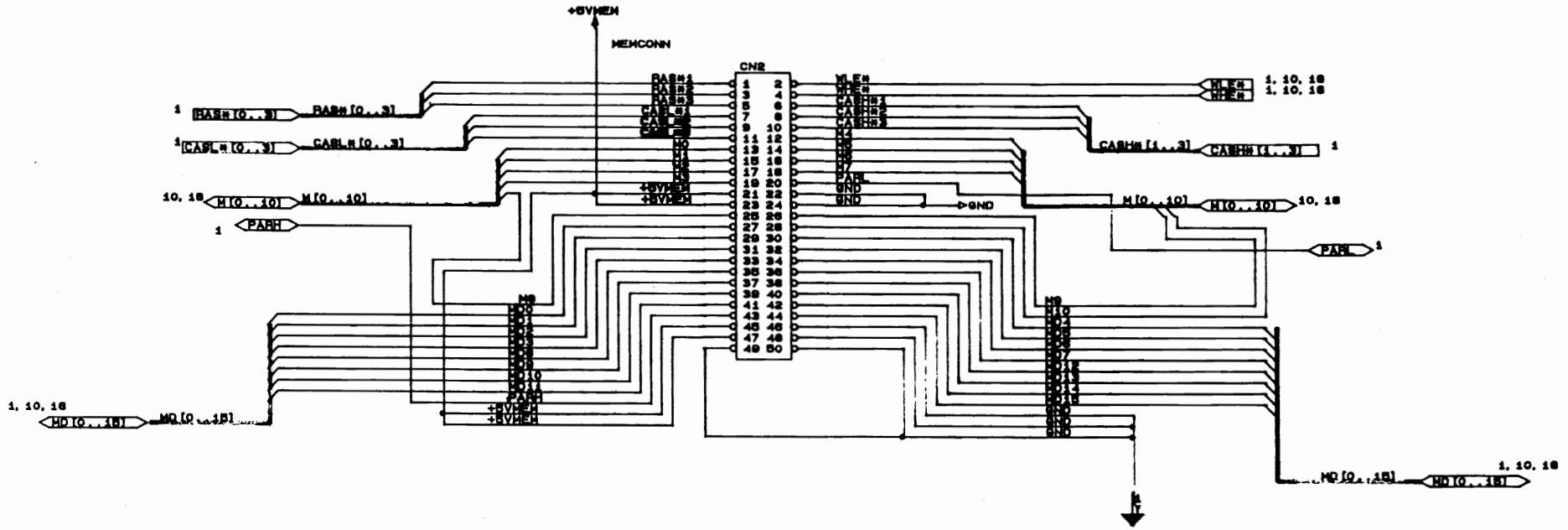

NOTE: EXITING FROM PWRON MODE.
THE PWROFF#S SHOULD BE ACTIVE FIRST, AFTER 100 mS THEN ACTIVATED THE PWROFF#S IN ORDER TO STABLIZE THE CLK INPUT.
NOTE: REFER TO INTEL SCHEMATICS.
NOTE: ANALOG PWR PLANE.
ANALOG GND PLANE.
FOR SEPERATING D AND A GND
NOTE:
1. 0.1UF SHOULD BE PLACED BETWEEN U10-9 AND U10-10 C38
U10-28 AND U10-27 C39
U10-53 AND U10-54 C106
U10-67 AND U10-66 C107
U10-94 AND U10-95 C108
2. PUT SOME VIA HOLES BETWEEN DIGITAL GND PLANE AND ANALOG GND PLANE. BETWEEN DIGITAL PWR PLANE AND ANALOG PWR PLANE
3. AT LEAST 1/8 INCH GAP BETWEEN TWO PLANES.
SAMSUNG PC Product Engineering Dept
Title
VGA SUBSYSTEM INTERFACE I (VGA1.SCH)
Size C
Document Number PENMASTER
REV A
Date: May 28, 1992 Sheet 8 of 20


U232
U231
TC511664
TC511664J
74AHCT74
74AHCT02
74AHCT04
74HCT05
LM324
+5VSYS
VCC
GND
+5VA
VLCD ON
LCD ON
LCD BUFF CON
CRT BUFF CON
LCDFR
VCONTRAST
PWR8000
VHD[0..15]
VHA[0..7]
LD[0..3]
UD[0..3]
SD[0..15]
LCDFP
LCDLP
LCDXSCLK
HSYNC
VSYNC
BLUE
GREEN
RED
CRTGND
LCDGND
LCD CONNECTOR
15 PIN VGA CONNECTOR
NOTE: VLCD SHOULD BE BIGGER TRACE.
NOTE: ANALOG PWR PLANE.
ANALOG GND PLANE.
SAMSUNG PC Product Engineering Dept
VGA SUBSYSTEM INTERFACE II (VGA2.SCH)
PENMASTER
May 28, 1992 Sheet 7 of 20

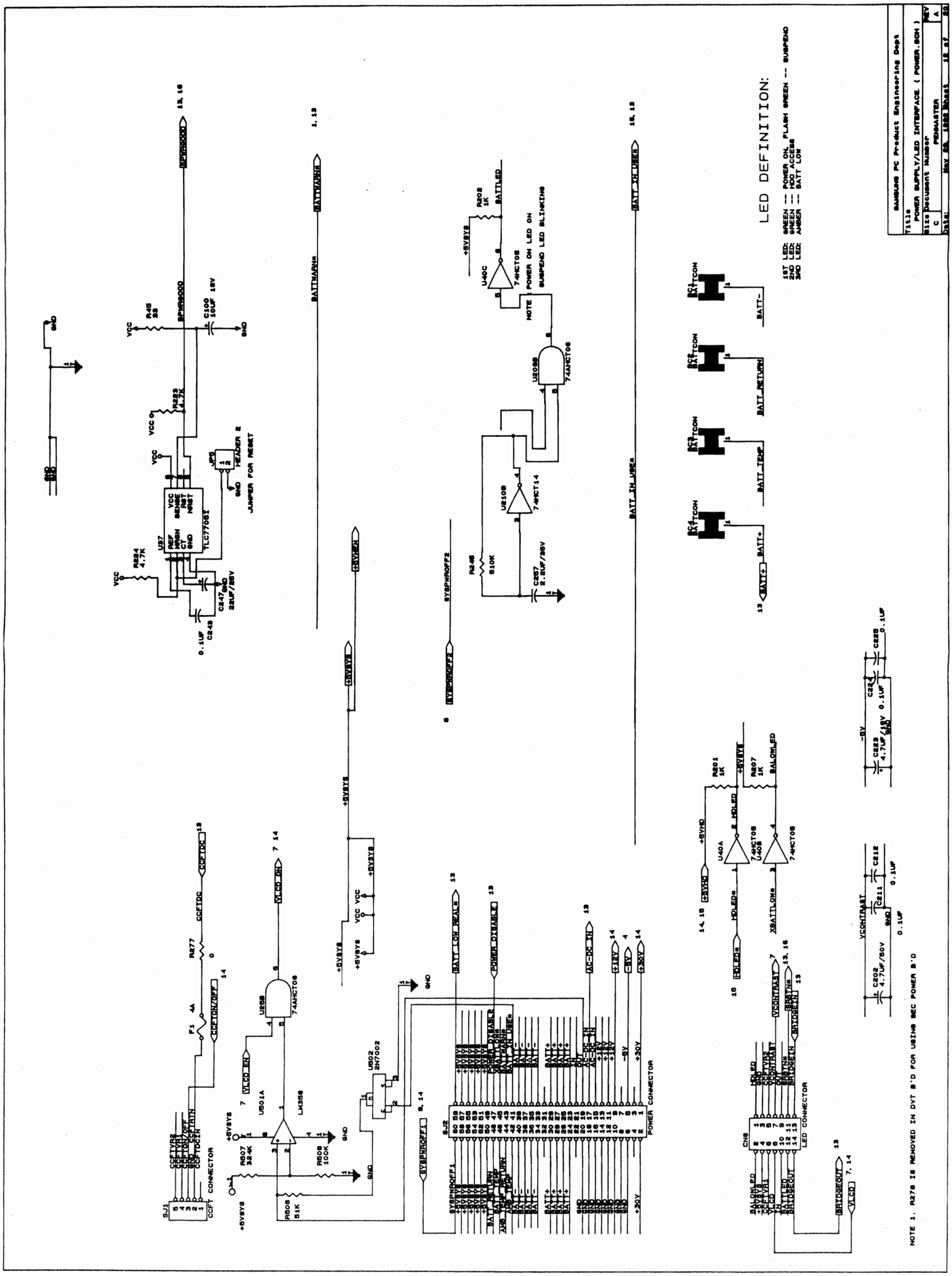

NOTE: 1-2 +5VSYS DEFAULT
2-3 SYSTEMVCC
NOTE: TAKE OUT R46 FOR STEP B
PIN 7, 8, 9 IS CONNECTED TO KGND
PS2 KBD CONNECTOR
SAMSUNG PC Product Engineering Dept
Title
KEYBD (NOTE1A.SCH)
Size C
Document Number
PENMASTER
REV A
Date: May 28, 1992 Sheet 8 of 20

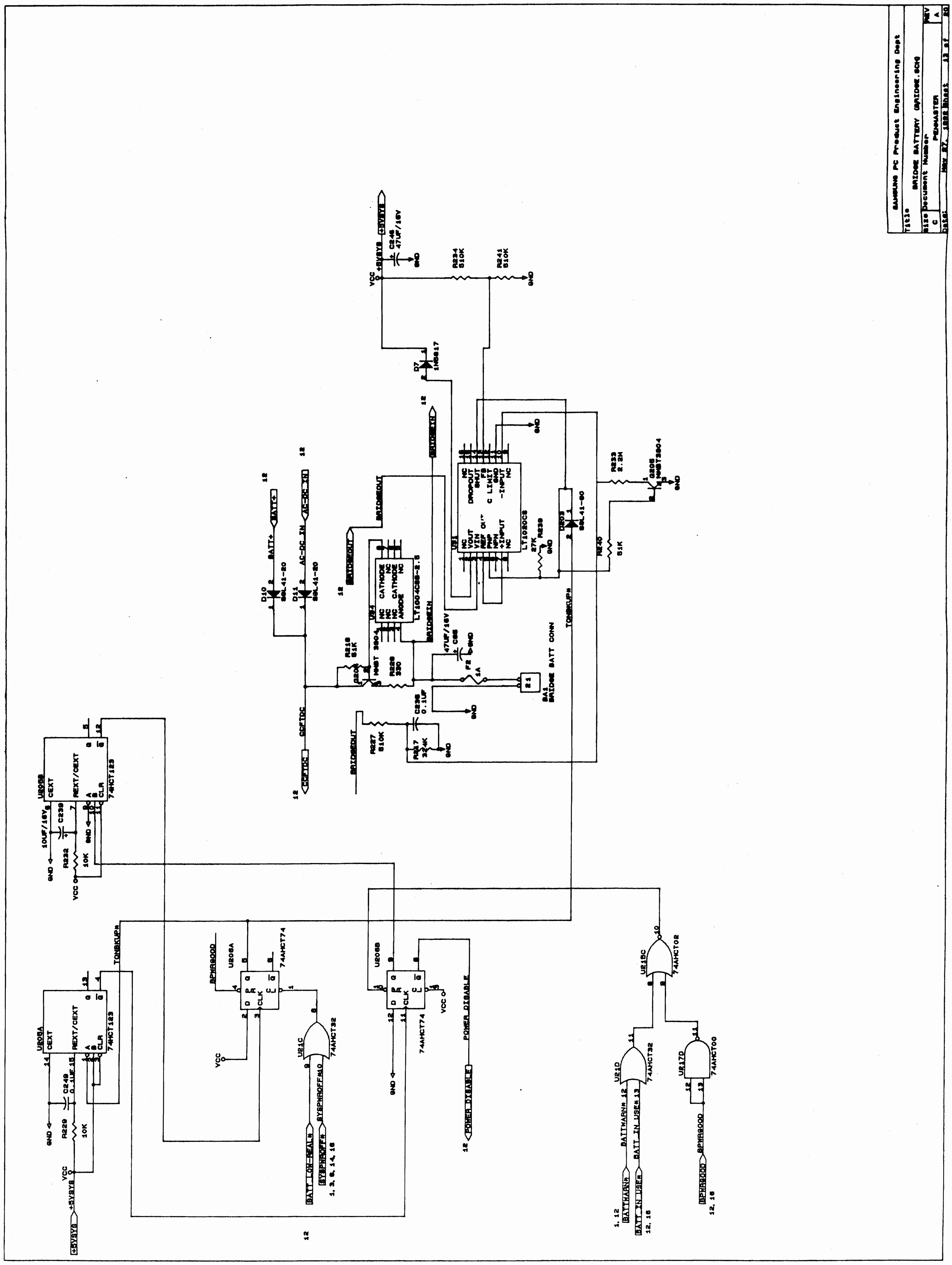

+5VSYS
U23
27C010
XD[0..7]
SA[0..18]
SYSTEMVCC
CA[1..15]
U18
U17
SC8408
SHUNT 1 2 FOR 64K CACHE
SHUNT 2 3 FOR 16K CACHE
JP4
SMD 3P PAD
R252
10K
C287
0.1UF
C288
0.1UF
C300
0.1UF
U27
CPUCLK2
NUMCLK2
R250
330
R251
20K
C87
0.1UF
C286
0.1UF
C276
0.1UF
C284
0.1UF
803878X
NPXW/R#
NPXBUSY#
PEREQ
NPXRDY#
NPXADS#
NPXCLK
SAMSUNG PC Product Engineering Dept
Title
3878X, CACHE AND FLASH EPROM (NOTES.SCH)
Size C
Document Number
PENMASTER
REV A
Date: May 26, 1992 Sheet 8 of 20


SAMSUNG PC Product Engineering Dept
Title
2MB BASE MEMORY (NOTE3.SCH)
Size Document Number
C PENMASTER
REV
A
SAMSUNG KH44C1000J-8
U5
U6
U7
U8
VCC
+5VMEM
+5VSYS
C47 0.1UF
C48 0.1UF
C49 0.1UF
C50 0.1UF
C8 0.1UF
C4 0.1UF
MA[0..10]
M[0..10]
MD[0..15]

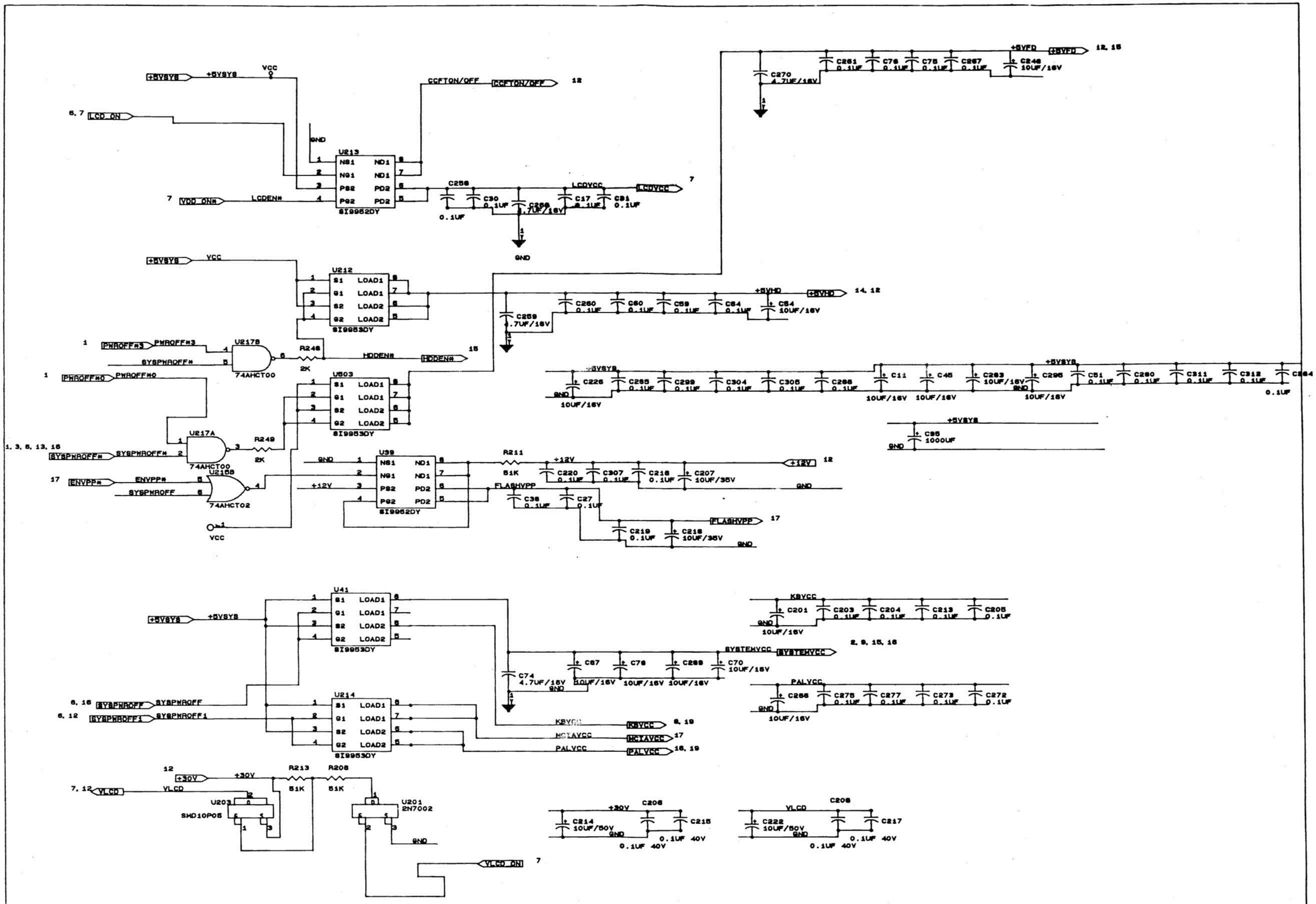


SAMSUNG PC Product Engineering Dept		
Title: MEMORY OPTION CONNECTOR (NOTE4A.SCH)		
Size: C	Document Number: PENMASTER	REV: A
Date: May 28, 1992	Sheet 11 of 20	

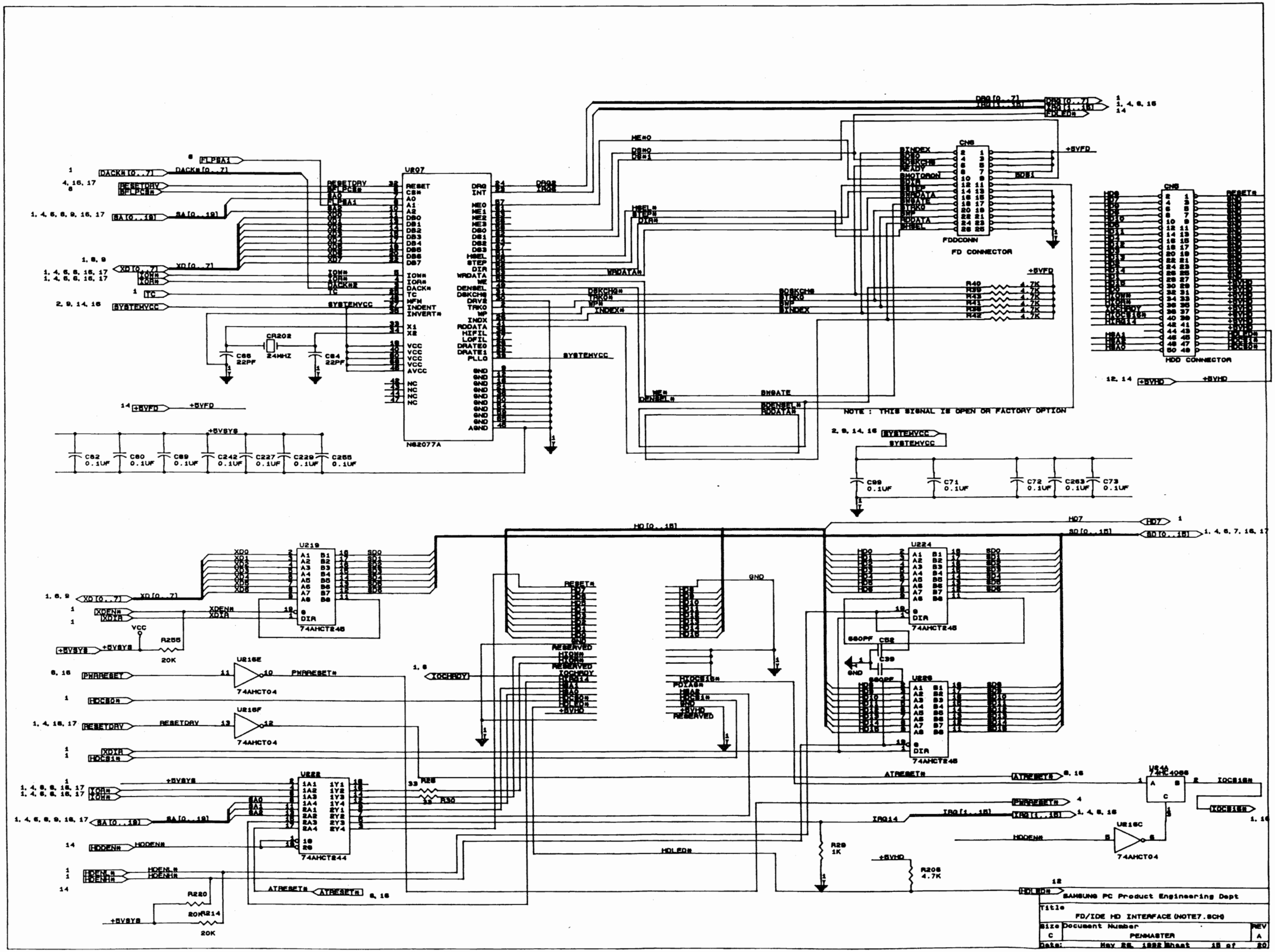

SAMSUNG PC Product Engineering Dept
Title
POWER SUPPLY/LED INTERFACE (POWER.SCH)
Size C
Document Number
PENMASTER
REV A
Date: May 20, 1992 Sheet 12 of 20
LED DEFINITION:
1ST LED: GREEN == POWER ON, FLASH GREEN -- SUSPEND
2ND LED: GREEN == HDD ACCESS
3RD LED: AMBER == BATT LOW
NOTE : POWER ON LED ON
SUSPEND LED BLINKING
BATT IN USE#
JUMPER FOR RESET
CCFT CONNECTOR
LED CONNECTOR
POWER CONNECTOR
NOTE 1. R278 IS REMOVED IN DVT B'D FOR USING SEC POWER B'D

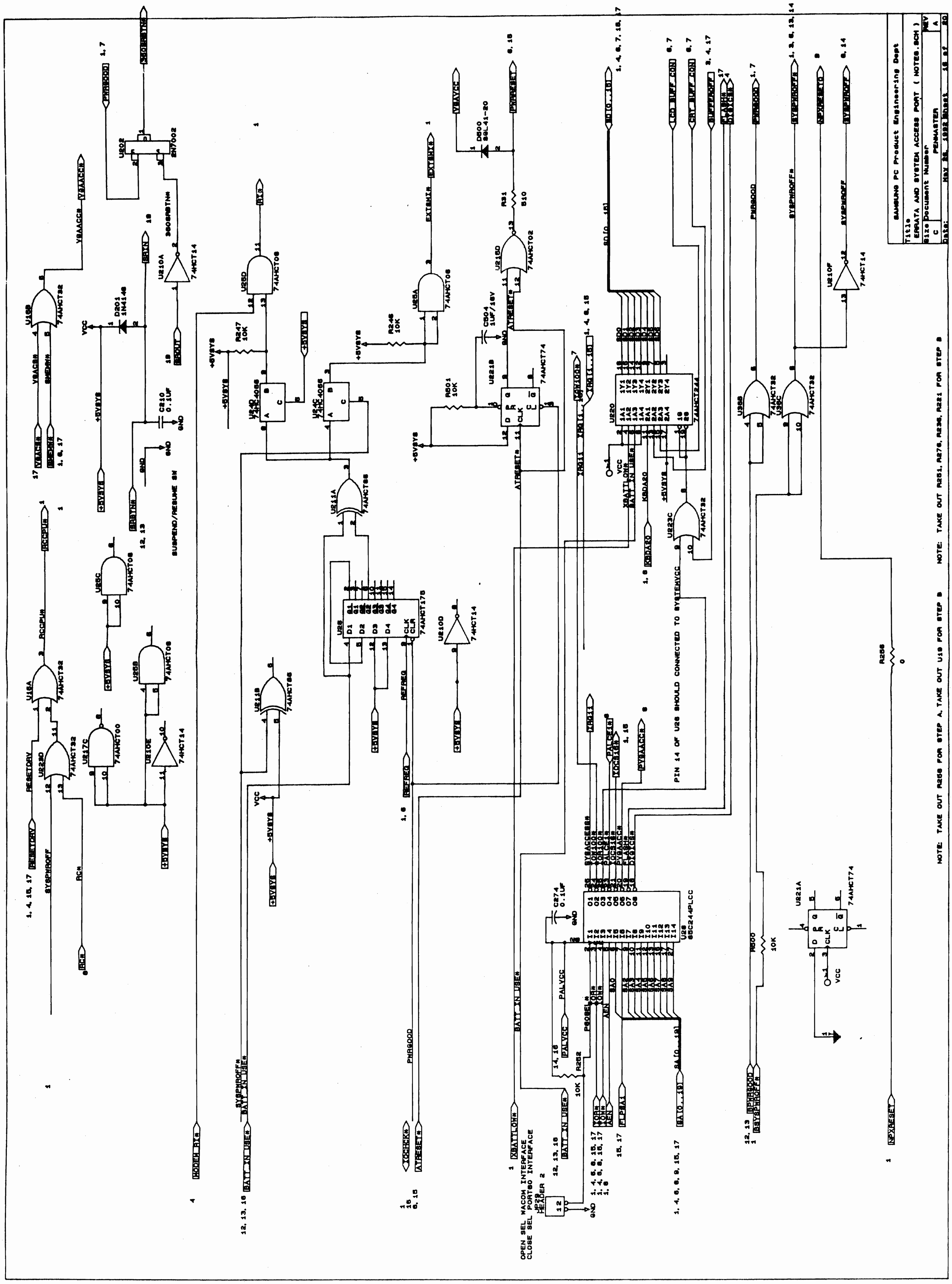


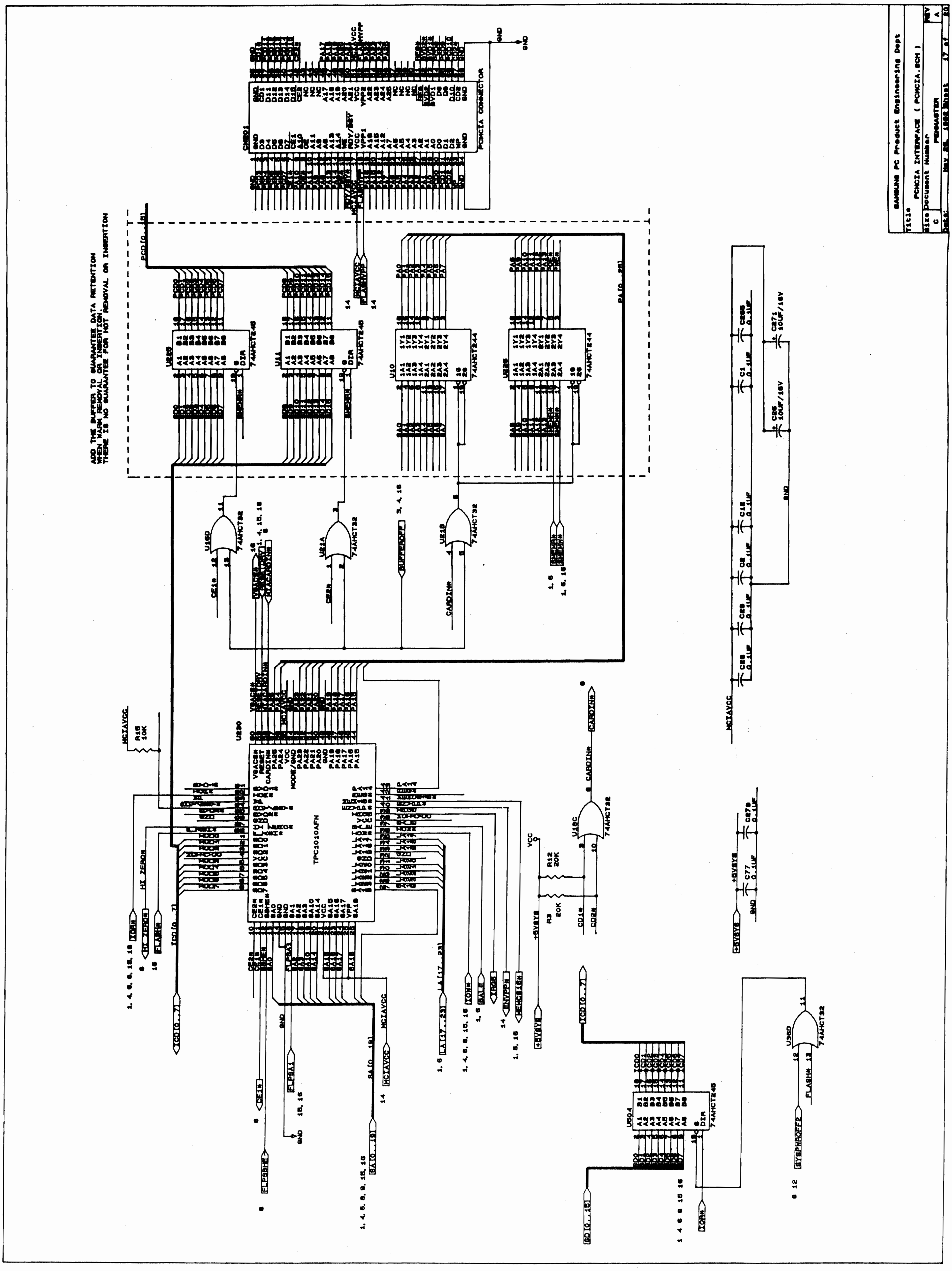
SAMSUNG PC Product Engineering Dept
Title BRIDGE BATTERY (BRIDGE.SCH)
Size C
Document Number PENMASTER
REV A
U205A 74HCT123
U205B 74HCT123
U206A 74AHCT74
U206B 74AHCT74
U21C 74AHCT32
U21D 74AHCT32
U215C 74AHCT02
U217D 74AHCT00
U31 LT1020CS
U34 LT1004CS8-2.5
D7 1N5817
D10 SGL41-20
D11 SGL41-20
D203 SGL41-60
Q205 MMBT3904
BA1 BRIDGE BATT CONN
F2 1A
R234 510K
R241 510K
R233 2.2M
R240 51K
R239 27K
R218 51K
R226 330
R227 510K
R229 10K
R232 10K
C246 47UF/16V
C85 47UF/16V
C236 0.1UF
C239 10UF/16V
BATT+
AC-DC IN
CCFTDC
BRIDGEIN
BRIDGEOUT
TONBKUP#
BPWRGOOD
POWER DISABLE
BATT LOW-REAL#
SYSPWROFF#
BATTWARN#
BATT IN USE#
+5VSYS
VCC
GND

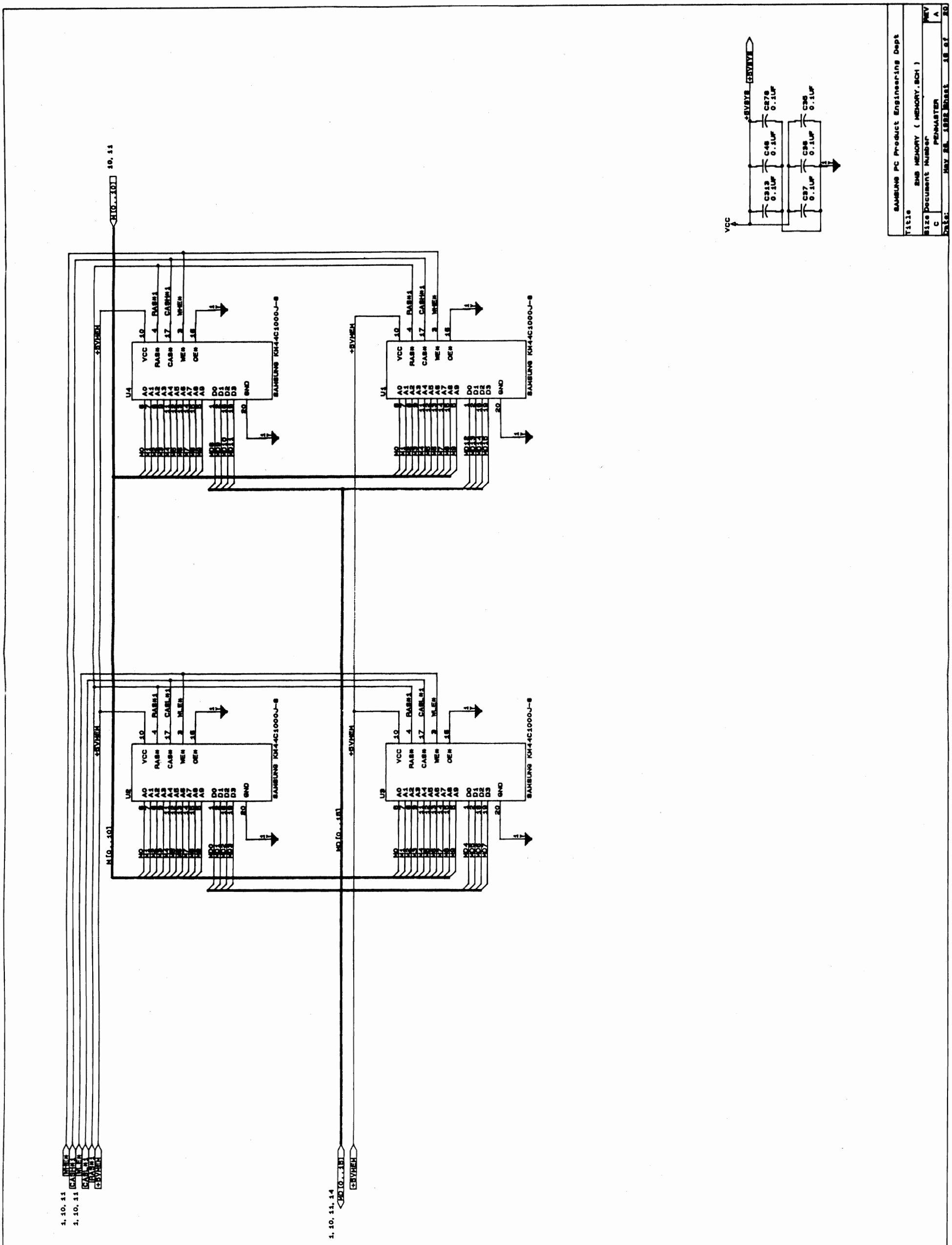


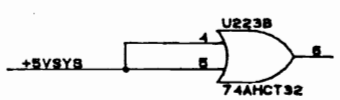
SAMSUNG PC Product Engineering Dept		
Title: POWER MANAGEMENT (NOTE8.SCH)		
Size: C	Document Number: PENMASTER	REV: A
Date: May 26, 1998	Sheet 14 of 20	

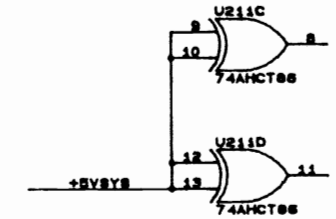

U207
NS2077A
RESETDRV
FLPCS#
FLPDA1
DACK#[0..7]
SA[0..19]
XD[0..7]
IOW#
IOR#
DACK#
TC
SYSTEMVCC
CR202
24MHZ
C85 22PF
C84 22PF
+5VFD
+5VSYS
C82 0.1UF
C80 0.1UF
C89 0.1UF
C242 0.1UF
C227 0.1UF
C229 0.1UF
C255 0.1UF
DRQ
INT
MEO
ME1
ME2
ME3
DS0
DS1
DS2
DS3
HSEL
STEP
DIR
WRDATA
WE
DENSEL
DSKCHG
DRV2
TRK0
WP
INDX
RDDATA
MFIL
LOFIL
DRATE0
DRATE1
PLLO
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
X1
X2
VCC
VCC
VCC
VCC
AVCC
NC
NC
NC
NC
AGND
DRQ[0..7]
IRQ[1..15]
ME#0
DS#0
DS#1
HSEL#
STEP#
DIR#
WRDATA#
DSKCHG#
TRK0#
WP#
INDEX#
WE#
DENSEL#
RDDATA#
CN8
FDDCONN
FD CONNECTOR
INDEX
DSKCHG
READY
MOTORON
DS1
DS0
WP#
RDDATA
STEP#
TRK0
DIR#
WRDATA
HDSEL
+5VFD
R40 4.7K
R39 4.7K
R43 4.7K
R41 4.7K
R38 4.7K
R42 4.7K
HDD CONNECTOR
RESET#
HDA1
HDA0
HDCS0#
HDCS1#
IOCHRDY
ACKDRQ3
HDRQ14
HDA2
+5VHD
NOTE : THIS SIGNAL IS OPEN OR FACTORY OPTION
SYSTEMVCC
C99 0.1UF
C71 0.1UF
C72 0.1UF
C263 0.1UF
C73 0.1UF
HD[0..15]
HD7
SD[0..15]
U219
U224
U229
74AHCT245
XDO
XD1
XD2
XD3
XD4
XD5
XD6
XD7
SDO
SD1
SD2
SD3
SD4
SD5
SD6
SD7
XDEN#
XDIR
VCC
R255 20K
RESERVED
IOCHRDY
HIOW#
HIOR#
HDACK3#
HDRQ14
HDCS0#
HDCS1#
+5VHD
POWERON#
GND
680PF C52
C39
U216E
U216F
74AHCT04
PWRRESET#
HDCS0#
RESETDRV
XDIR
U228
74AHCT244
IOW#
IOR#
SA[0..19]
HDDEN#
HDEN1#
HDEN0#
R220 20K
R214 20K
ATRESET#
R25 33
R30 33
IRQ14
R29 1K
R206 4.7K
U216C
U146
74HC4066
IOCS16#
SAMSUNG PC Product Engineering Dept
Title
FD/IDE HD INTERFACE (NOTE7.SCH)
Size C
Document Number PENMASTER
REV A
Date: May 26, 1992 Sheet 15 of 20

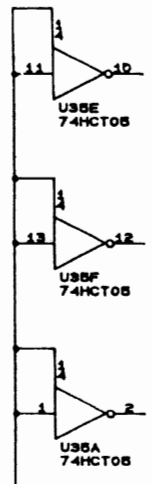

SAMSUNG PC Product Engineering Dept
Title
ERRATA AND SYSTEM ACCESS PORT (NOTES.SCH)
Size C Document Number PENMASTER REV A
Date: May 28, 1992 Sheet 18 of 20
NOTE: TAKE OUT R256 FOR STEP A, TAKE OUT U19 FOR STEP B
NOTE: TAKE OUT R251, R276, R236, R221 FOR STEP B
PIN 14 OF U26 SHOULD CONNECTED TO SYSTEMVCC
OPEN SEL WACOM INTERFACE
CLOSE SEL PORT80 INTERFACE

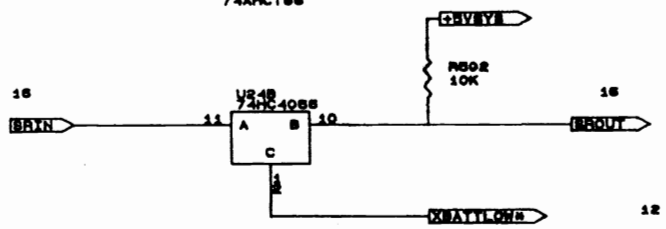

SAMSUNG PC Product Engineering Dept
Title
PCMCIA INTERFACE (PCMCIA.SCH)
Size C
Document Number
PENMASTER
REV A
Sheet 17 of 20
ADD THE BUFFER TO GUARANTEE DATA RETENTION
WHEN WARM REMOVAL OR INSERTION.
THERE IS NO GUARANTEE FOR HOT REMOVAL OR INSERTION
PCMCIA CONNECTOR
TPC1010AFN
74AHCT245
74AHCT244
74AHCT32
U504
CARDIN#
MCIAVCC
+5VSYS
R12 20K
R3 20K
R15 10K

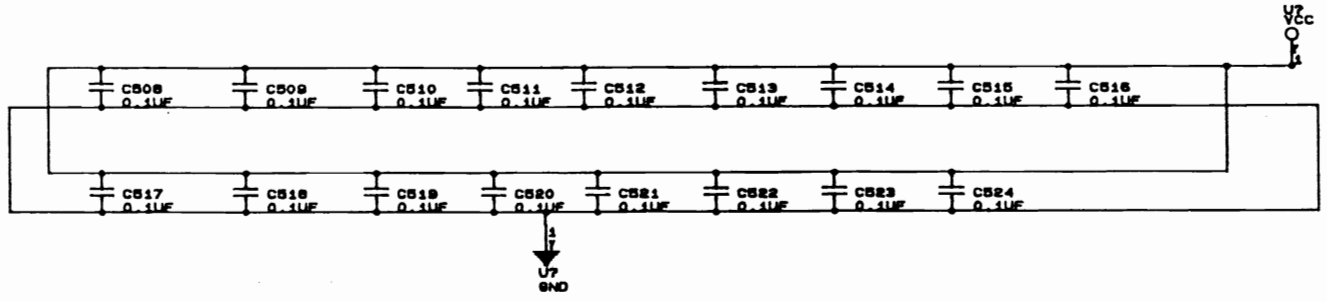

SAMSUNG PC Product Engineering Dept
Title
8MB MEMORY (MEMORY.SCH)
Size
C
Document Number
PENMASTER
REV
A
Date:
May 28, 1992 Sheet
18 of
20
+5VSYS
C279 0.1UF
C48 0.1UF
C313 0.1UF
C36 0.1UF
C35 0.1UF
C37 0.1UF
VCC
+5VMEM
MA[10..1]
MD[0..16]
SAMSUNG KM44C1000J-8
U1
U2
U3
U4
1, 10, 11
1, 10, 11, 14

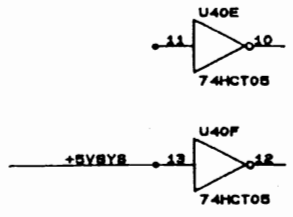




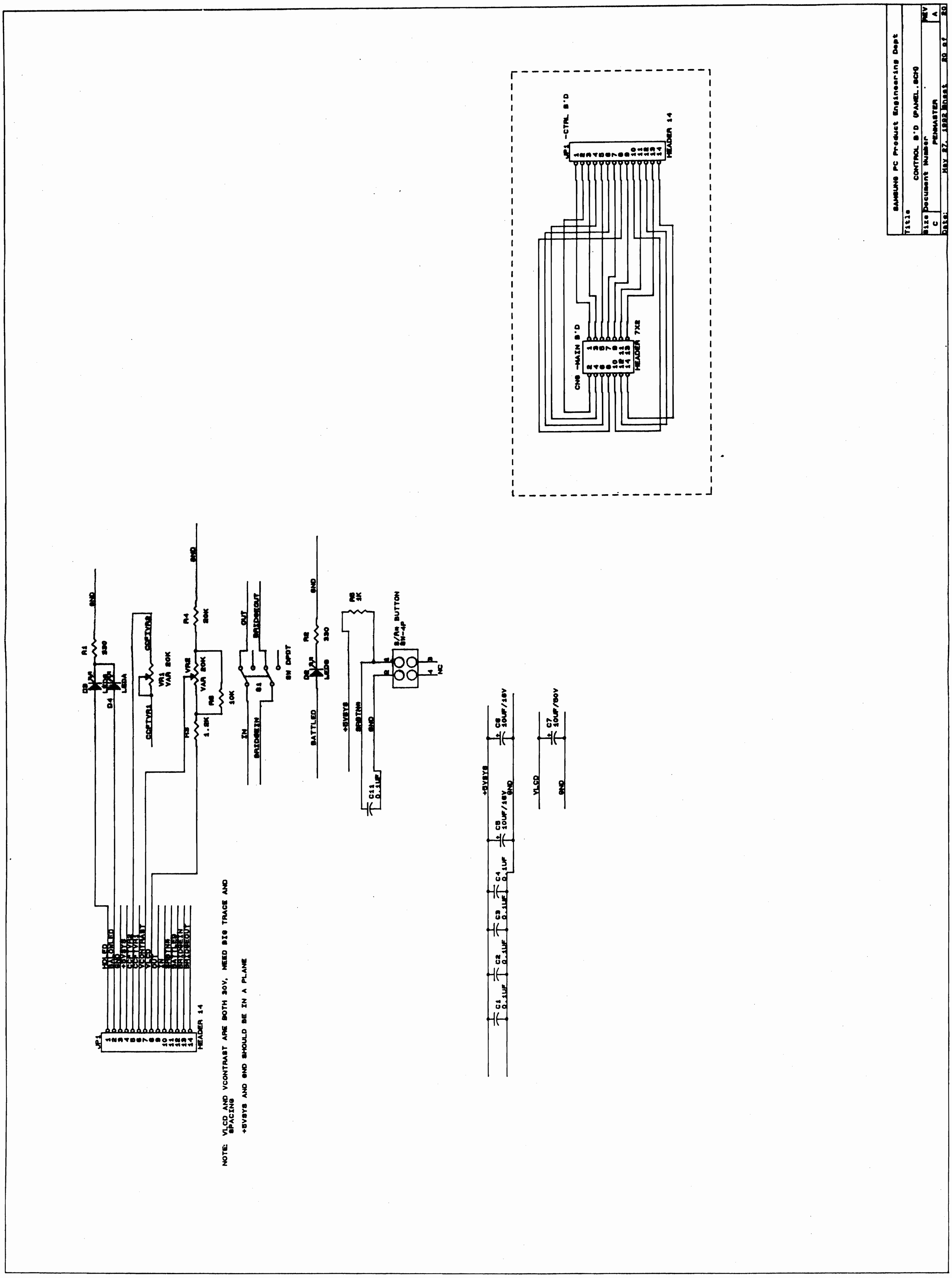




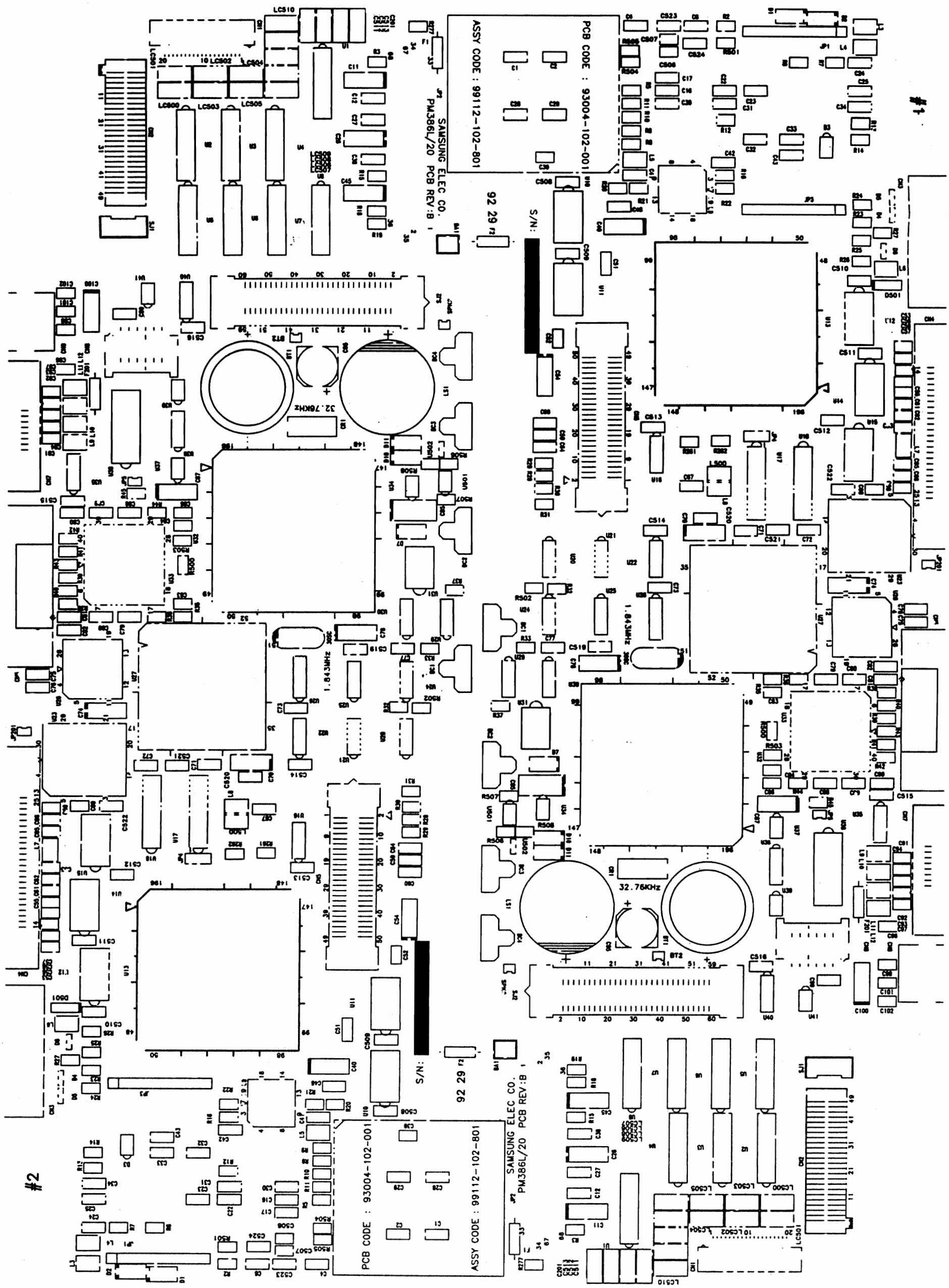




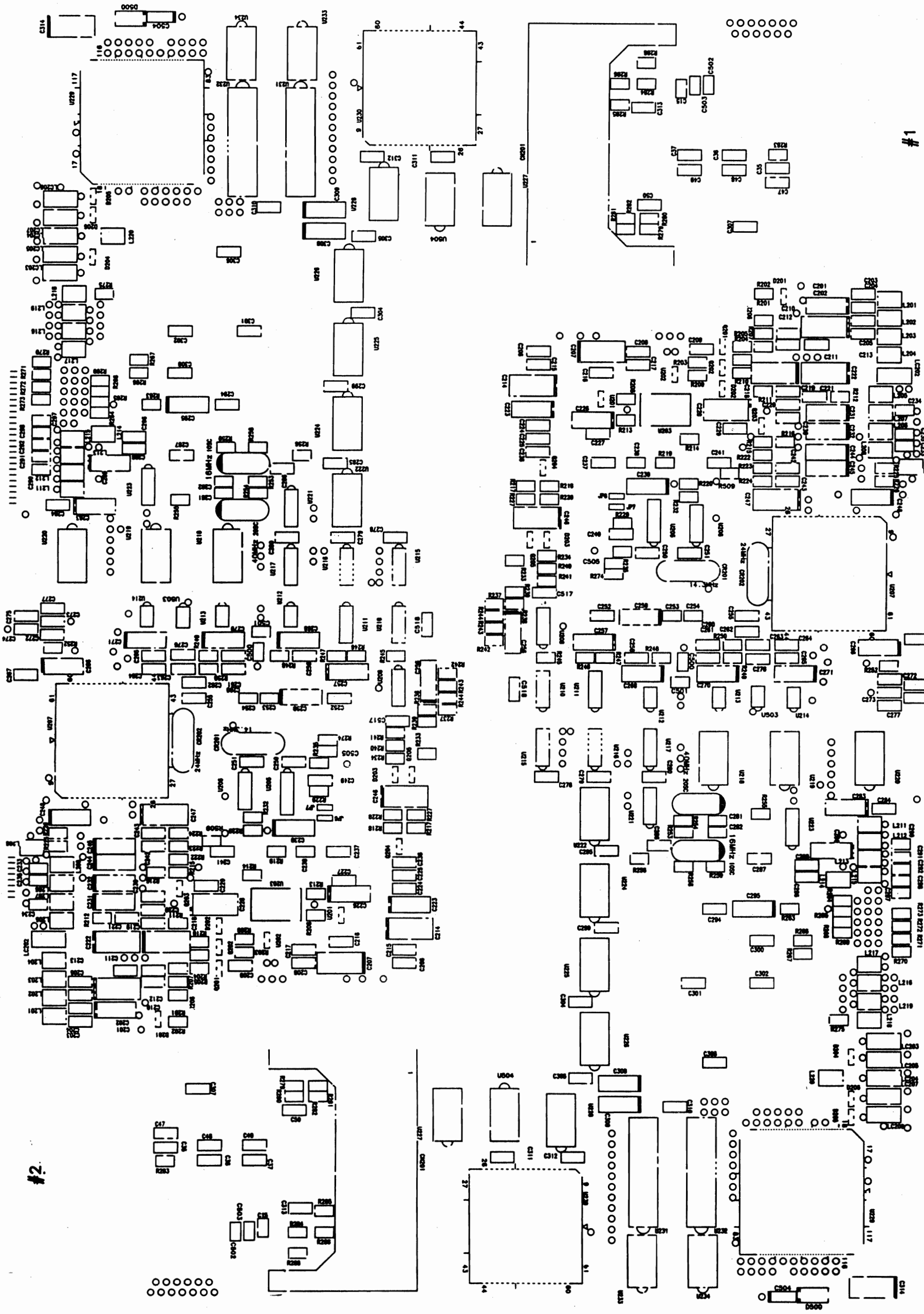
SAMSUNG PC Product Engineering Dept		
Title: UNUSED PARTS (UNUSED.SCH)		
Size: C	Document Number: PENMASTER	REV: A
Date: May 28, 1992	Sheet 18 of 20	


JP1
HEADER 14
HDLED
BALOWLED
GND
+5VSYS
CCFTVR2
CCFTVR1
VCONTRAST
VLCD
OUT
IN
SEBTNN
BATTLED
BRIDGEIN
BRIDGEOUT
NOTE: VLCD AND VCONTRAST ARE BOTH 30V, NEED BIG TRACE AND SPACING
+5VSYS AND GND SHOULD BE IN A PLANE
D3
D4
LEDA
R1
330
VR1
VAR 20K
CCFTVR1
CCFTVR2
R3
1.2K
R5
10K
VR2
VAR 20K
R4
20K
S1
SW DPDT
D5
LEDG
R2
330
R6
1K
S/R BUTTON
SW-4P
NC
C11
0.1UF
C1
0.1UF
C2
0.1UF
C3
0.1UF
C4
0.1UF
C5
10UF/16V
C6
10UF/16V
C7
10UF/50V
CN6 -MAIN B'D
HEADER 7X2
JP1 -CTRL B'D
HEADER 14
SAMSUNG PC Product Engineering Dept
Title
CONTROL B'D (PANEL.SCH)
Size
C
Document Number
PENMASTER
REV
A
Date:
May 27, 1992
Sheet
20 of
20

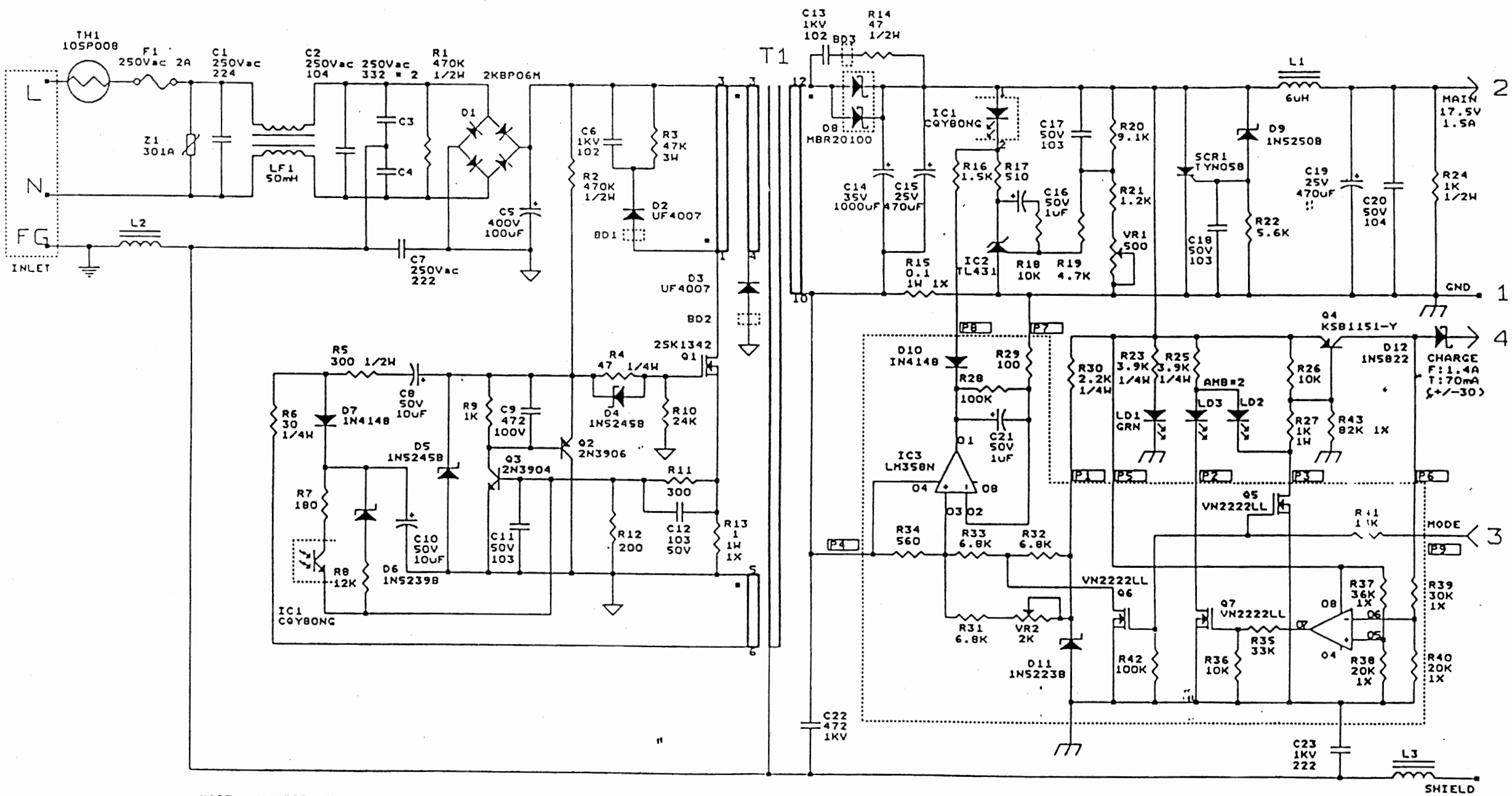
M/K-01


#1
#2
PCB CODE : 93004-102-001
ASSY CODE : 99112-102-801
SAMSUNG ELEC CO.
PM386L/20 PCB REV:B 1
92 29
S/N:
32.768KHz
1.843MHz

M/K-08



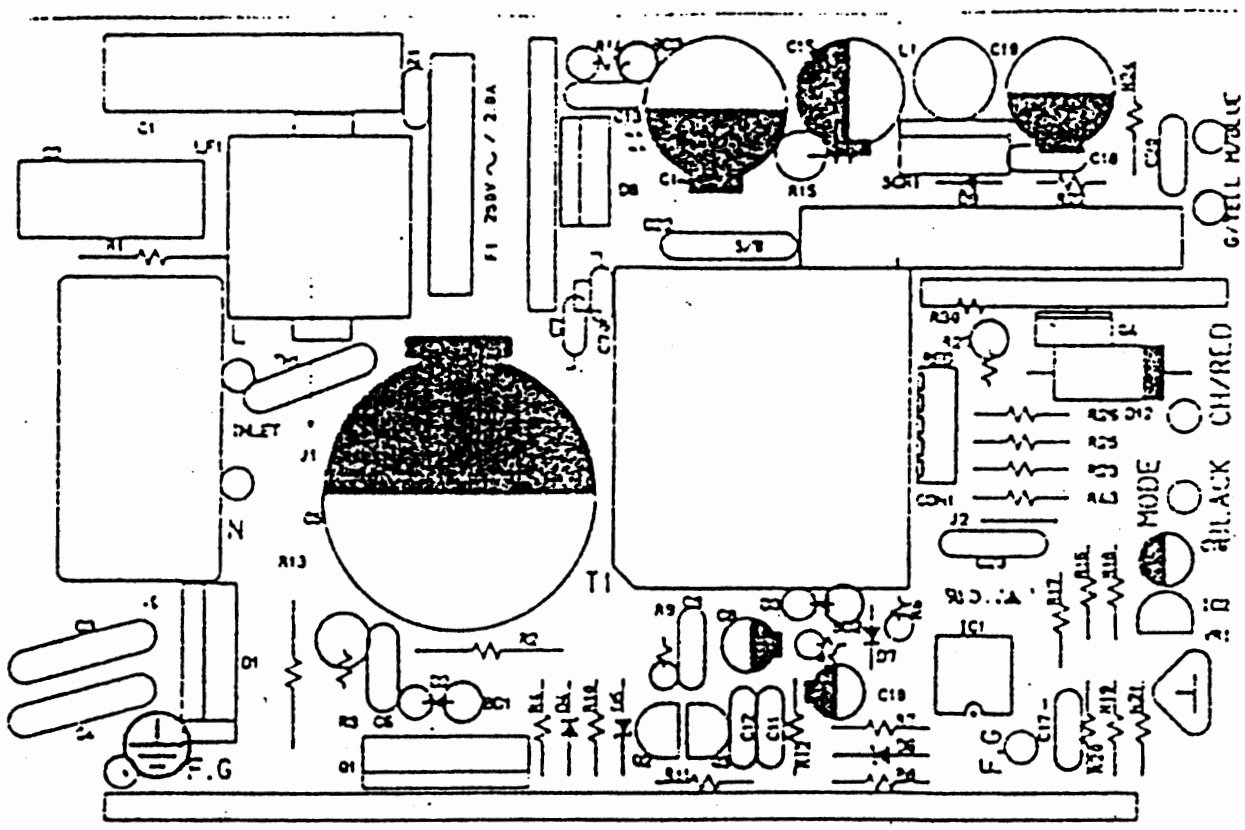
CIRCUIT DIAGRAM (AC ADAPTER)



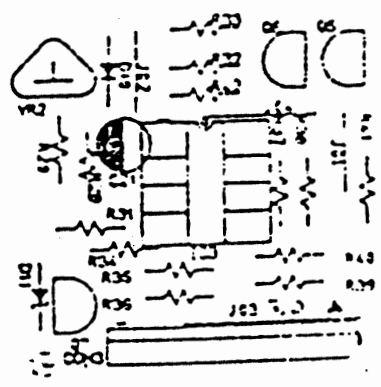
NOTE : UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE
IN OHMS , 1/8W , 5%.

FILENAME : AD-26A		
Size B	Document Number DFG AD-26	REV 1.1
Date: June 10, 1992	Sheet 1 of 1	

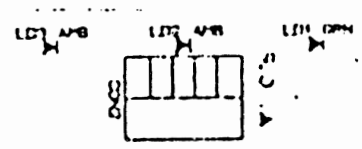
COMPONANTS SIDE & PATTERN DRAWING OF PWB (AC ADAPTER)



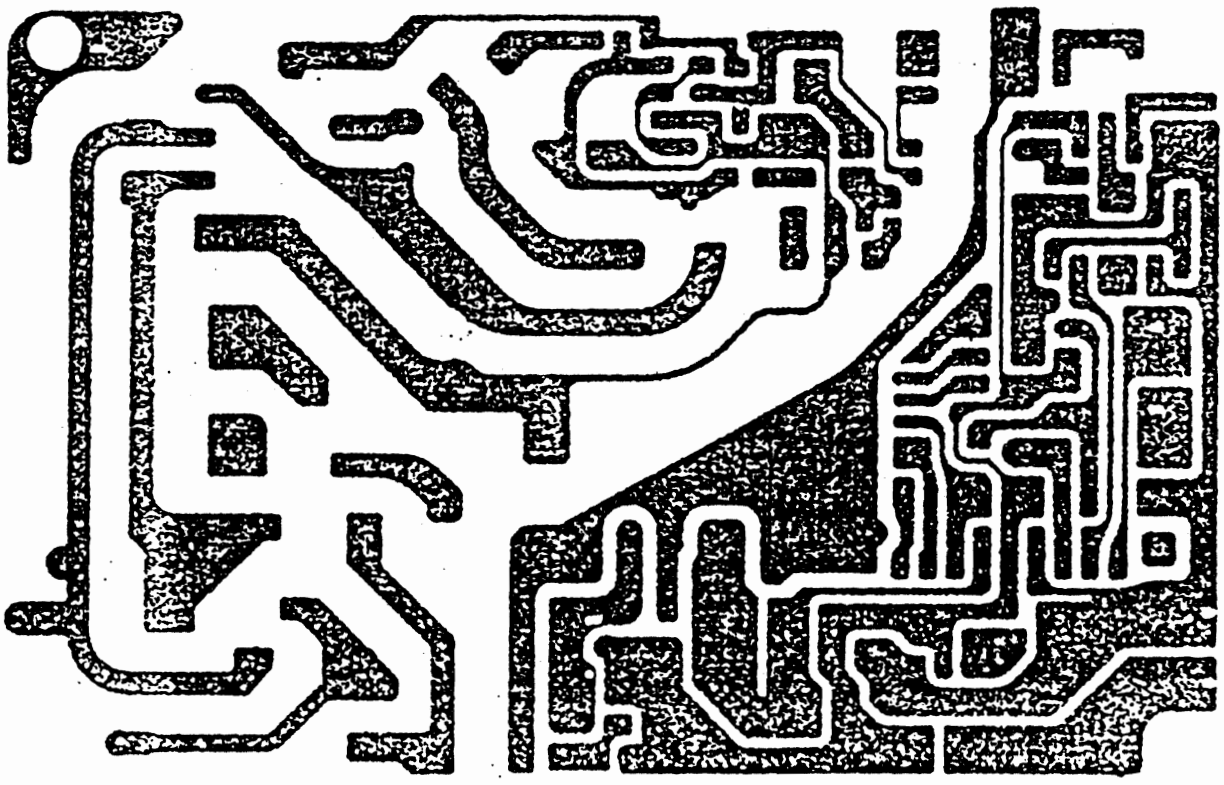
PCB-MAIN COMPONENT



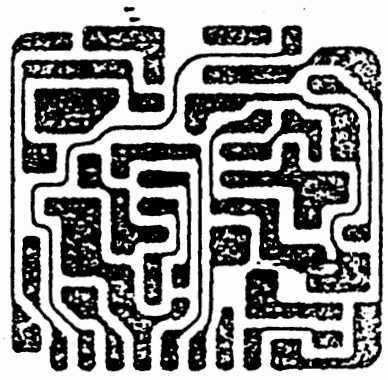
PCB-SUB COMPONENT



PCB-LED COMPONENT



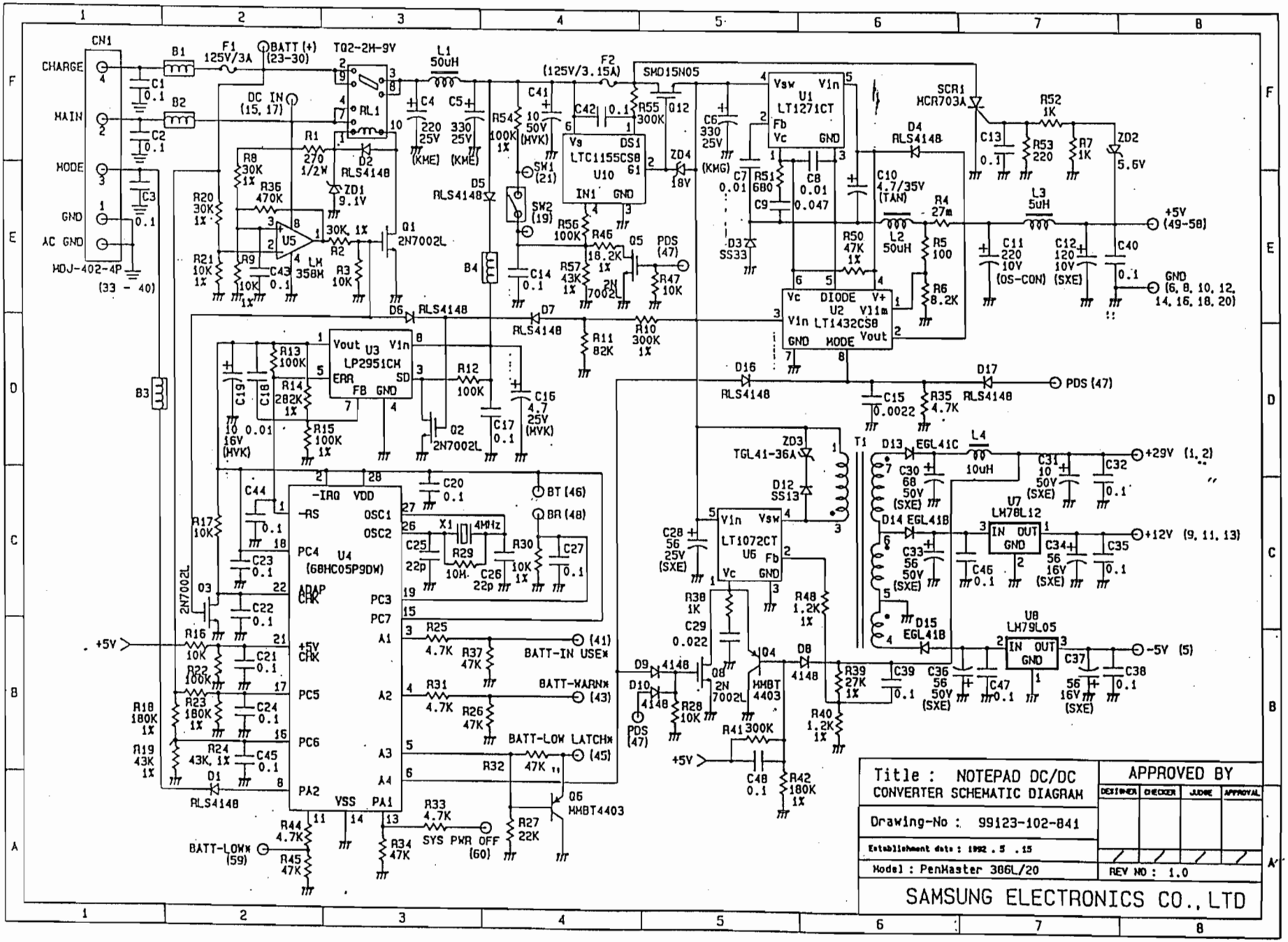
PCB-MAIN PATTERN



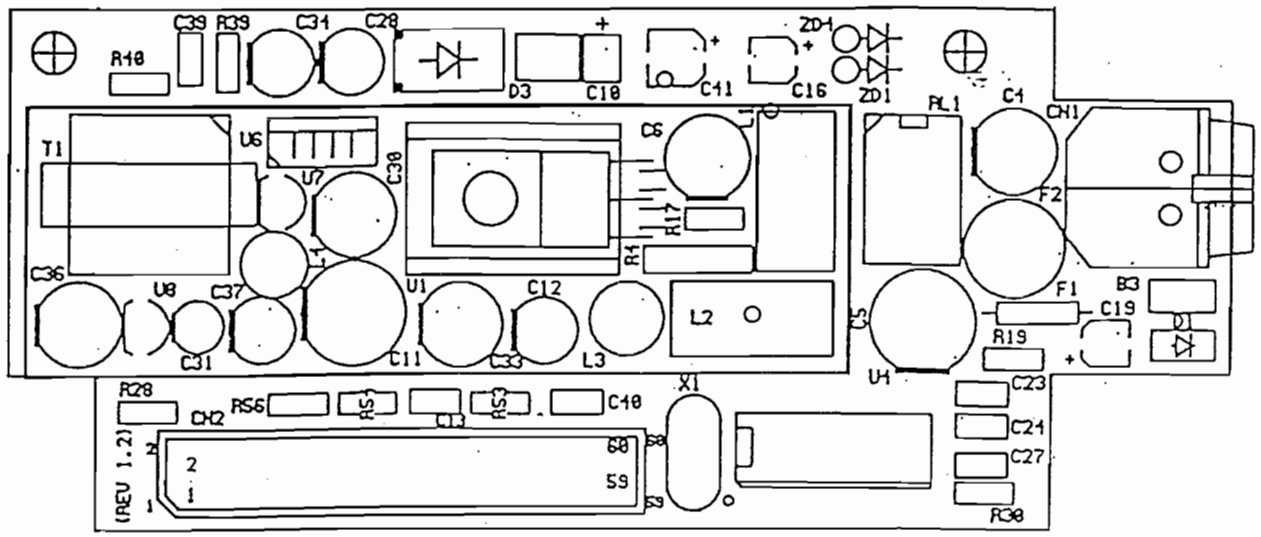
PCB-SUB PATTERN

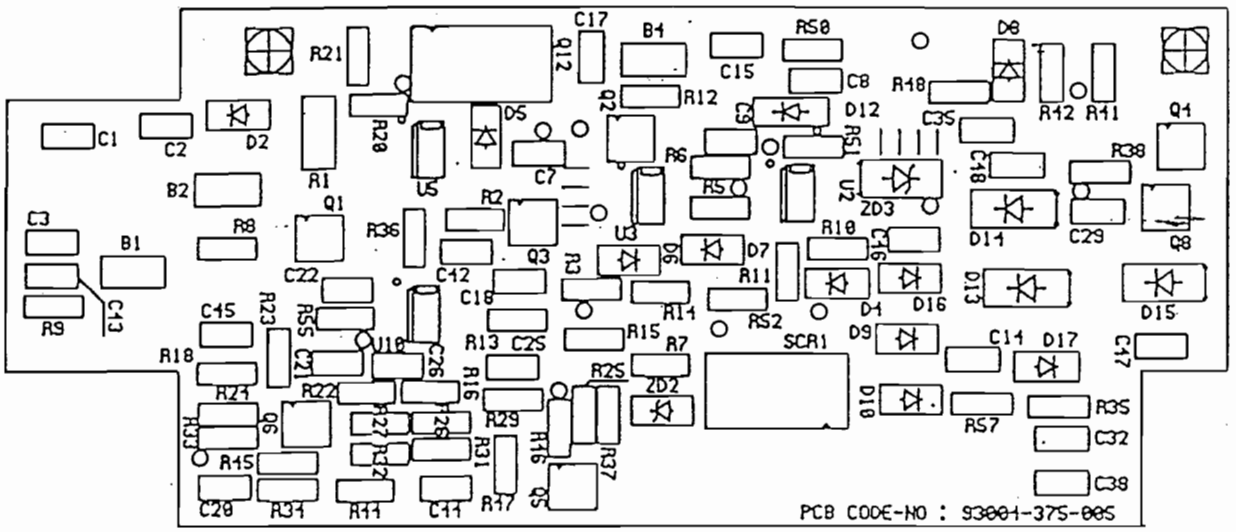
PCB-LED PATTERN

CIRCUIT DIAGRAM (DC/DC CONVERTER)



COMPONENTS SIDE OF PWB (DC/DC CONVERTER B'D)





Appendix B

Parts List

A. MECHANICAL PARTS LIST

LEVEL	PART NUMBER	DESCRIPTION	SPECIFICATION	CC	REF-DESN	QTY
.1	99101-102-020	ASSY-BOTTOM (SEC)	NOTEPAD1			1
..2	95904-903-010	INSULATOR	DC/DC PWR ,PVC T=0.3			2
..2	96031-902-020	HOUSING	BOTTOM-HOU ,PC/ABS			1
..2	97641-900-120	DOOR	BATTERY ,PC/ABS			1
..2	97641-900-220	DOOR	LEFT I/O ,THERMOPLA			1
..2	97641-900-320	DOOR	RIGHT I/O ,THERMOPLA			1
..2	97641-900-420	DOOR	POWER JACK ,THERMOPLA			1
..2	98114-001-030	LABEL-BARCODE	SET,55*12 ,ALL MODEL			1
..2	98114-375-036	LABEL-ID	SAMSUNG ,NOTEPAD1			1
..2	98464-907-830	FOOT	RUBBER ,NEOPRENE			4
.1	99102-102-020	ASSY-TOP (SEC)	NOTEPAD1			1
..2	96051-970-720	COVER-ASSY	TOP-HOUSING ,PC/ABS			1
..2	96052-904-710	PANEL	DUMMY IC ,PC/ABS			1
..2	96602-900-720	HOLDER	HOLDER-PEN ,THERMOPLA			2
..2	97621-900-020	KNOB	POWER ,PC/ABS			1
..2	97621-900-120	KNOB	CONTRAST ,PC/ABS			1
..2	97621-900-320	KNOB	BRIGHTNESS ,PC/ABS			1
..2	97652-900-110	LENS	LED ,ACRYL			1
..2	97694-900-110	BADGE	LOGO SEC ,ELECTRO C			1
..2	98704-905-310	SPONGE	GASKET LCD ,SPONGE			2

B. ELECTRICAL PARTS LIST

LEVEL	PART NUMBER	DESCRIPTION	SPECIFICATION	CC	REF-DESN	QTY
.1	99112-102-801	ASSY-MOTHER B/D	NOTEPAD1 MAIN B'D			1
..2	91083-000-751	R-CARBON CHIP	0 ,5% ,1/10W ,C		R233,256,277	3
..2	91083-102-750	R-CARBON CHIP	1K ,5% ,1/10W ,C	01	R29,37,201,202	
				02	R207	
					* Total Qty ===>	5
..2	91083-103-750	R-CARBON CHIP	10K ,5% ,1/10W ,C	01	R13-15,44,204	
				02	R210,222,229,232	
				03	R239,242,246,247	
				04	R259,253,259,262	
				05	R263,266,500,501	
				06	R509	
					* Total Qty ===>	22
..2	91083-104-750	R-CARBON CHIP	100K ,5% ,1/10W ,C		R2,R219,R508	3
..2	91083-151-750	R-CARBON CHIP	150 ,5% ,1/10W ,C		R24,25,27,212	4
..2	91083-153-750	R-CARBON CHIP	15K ,5% ,1/10W ,C		R5,8-11,33	6
..2	91083-202-750	R-CARBON CHIP	2K ,5% ,1/10W ,C		R248,249	2
..2	91083-203-750	R-CARBON CHIP	20K ,5% ,1/10W ,C	01	R3,12,214,220	
				02	R225,261	
					* Total Qty ===>	6
..2	91083-220-710	R-CARBON CHIP	22 ,1% ,1/10W ,C	01	R18,19,279-286	
				02	R288	
					* Total Qty ===>	11
..2	91083-221-710	R-CARBON CHIP	220 ,1% ,1/10W ,C		R7	1
..2	91083-223-750	R-CARBON CHIP	22K ,5% ,1/10W ,C		R243	1
..2	91083-225-750	R-CARBON CHIP	2.2M ,5% ,1/10W ,C		R233	1
..2	91083-273-750	R-CARBON CHIP	27K ,5% ,1/10W ,C		R203,239	2
..2	91083-302-750	R-CARBON CHIP	3K ,5% ,1/10W ,C		R244	1
..2	91083-323-710	R-CARBON CHIP	324K ,1% ,1/10 ,C		R217.R507	2
..2	91083-330-750	R-CARBON CHIP	33 ,5% ,1/10W ,C	01	R16,22,23,26,28	
				02	R30,45,209,254	
				03	R258,264,265	
				04	R268-275,505	
					* Total Qty ===>	21
..2	91083-331-750	R-CARBON CHIP	330 ,5% ,1/10W ,C		R228,250	2
..2	91083-430-750	R-CARBON CHIP	43 ,5% ,1/10W ,C		R216	1
..2	91083-470-751	R-CARBON CHIP	47 ,5% ,1/10W ,C		R35	1
..2	91083-472-750	R-CARBON CHIP	4.7K ,5% ,1/10W ,C	01	R32,36,38-43	
				02	R206,223-226	
				03	R235,267	
					* Total Qty ===>	15

LEVEL	PART NUMBER	DESCRIPTION	SPECIFICATION	CC	REF-DESN	QTY
..2	91083-511-750	R-CARBON CHIP	510 ,5% ,1/10W ,C		R31,238	2
..2	91083-513-750	R-CARBON CHIP	51K ,5% ,1/10W ,C	01	R6,205,208,211	
				02	R213,218,240	
				03	R506	
					* Total Qty ===>	8
..2	91083-514-750	R-CARBON CHIP	510K ,5% ,1/10W ,C		R227,234,241,245	4
..2	91083-515-750	R-CARBON CHIP	5.1M ,5% ,1/10W ,C		R233	1
..2	91083-682-710	R-CARBON CHIP	6.8K ,1% ,1/10W ,C		R503,504	1
..2	91083-750-710	R-CARBON CHIP	75 ,1% ,1/10W ,C		R20,21	2
..2	91083-822-751	R-CARBON CHIP	8.2K ,5% ,1/10W ,C		R215,237	2
..2	91301-102-751	C-CERAMIC CHIP	1nF ,5% ,50V ,N	01	C15,502,503	
				02	C281	
					* Total Qty ===>	4
..2	91301-103-251	C-CERAMIC CHIP	10nF ,5% ,50V ,X		C282	1
..2	91301-104-310	C-CERAMIC CHIP	0.1uF ,10% ,50V ,X	01	C1,2,4,6,12,16	
				02	C17,22-25,27-38	
				03	C41-43,46-51,59,	
				04	C60,64,67,71,72	
				05	C73,75-77,79-82	
				06	C88-90,99	
				07	C203-206,208-213	
				08	C215-217,219-221	
				09	C224,225,227,229	
				10	C230,236,237	
				11	C241-243,249-252	
				12	C255,258,260-265	
				13	C267,272-280	
				14	C284-288,294,296	
				15	C300-302,304-307	
				16	C310-313	
				17	C299,508-524	
					* Total Qty ===>	134
..2	91301-220-751	C-CERAMIC CHIP	22pF ,5% ,50V ,N		C84,86	2
..2	91301-271-751	C-CERAMIC CHIP	270pF ,5% ,50V ,N	01	C53,55-58,61-63	
				02	C65,66,68,69	
				03	C91-94,97	
				04	C233-235,290-292	
				05	C297,298	
					* Total Qty ===>	25
..2	91301-330-740	C-CERAMIC CHIP	33pF ,5% ,100V ,N		C253,254,500,501	2
..2	91301-470-640	C-CERAMIC CHIP	47pF ,2% ,100V ,N		C96,505-507	4
..2	91301-510-750	C-CERAMIC CHIP	51pF ,5% ,50V ,N		C238	1

LEVEL	PART NUMBER	DESCRIPTION	SPECIFICATION	CC	REF-DESN	QTY
..2	91301-681-750	C-CERAMIC CHIP	680pF ,5% ,50V ,N		C39,52	2
..2	91302-121-751	C-CERAMIC CHIP	120pF ,5% ,50V ,N		C98,101,102	3
..2	91311-102-130	C-ELECTRONIC	, , ,		C95	1
..2	91629-105-640	C-TANTAL CHIP	1uF ,10% ,16V ,G		C504	1
..2	91629-106-340	C-TANTAL CHIP	10uF ,10% ,35V ,G		C207,218,228	3
..2	91629-106-530	C-TANTAL CHIP	10uF ,10% ,50V ,G		C214,222	2
..2	91629-106-640	C-TANTAL CHIP	10uF ,10% ,16V ,G	01	C11,26,45,54,70	
				02	C78,87,201,226	
				03	C231,232,239,248	
				04	C256,266,271,283	
				05	C289,295,100	
					* Total Qty ===>	20
..2	91629-225-330	C-TANTAL CHIP	2.2uF ,10% ,35V ,G	01	C40,257,308	
				02	C309	
					* Total Qty ===>	4
..2	91629-226-240	C-TANTAL CHIP	22uF ,10% ,25V ,G		C247,314	2
..2	91629-475-530	C-TANTAL CHIP	4.7uF ,10% ,16V ,G	01	C74,223,244,245	
				02	C259,268,270	
					* Total Qty ===>	7
..2	91629-475-531	C-TANTAL CHIP	4.7uF ,10% ,50V ,G		C202	1
..2	91629-476-640	C-TANTAL CHIP	47uF ,10% ,16V ,G		C85,C246	2
..2	92109-620-050	IC-MOS	74HCT05 SOP-14		U35,40	2
..2	92109-620-140	IC-MOS	74HCT14 ,SOP-14		U210	1
..2	92109-620-860	IC-MOS	74HCT86 ,SOP-14		U211	1
..2	92109-621-230	IC-MOS	74HCT123 ,SOP-14		U205	1
..2	92109-630-001	IC-MOS	74ACT00 SOP-14		U20,217	2
..2	92109-630-020	IC-MOS	74ACT02 ,SOP-14		U215	1
..2	92109-630-040	IC-MOS	74ACT04 SOP-14		U216	1
..2	92109-630-080	IC-MOS	74ACT08 ,SOP-14		U22,25,208	3
..2	92109-630-320	IC-MOS	74ACT32 ,SOP-14		U16,21,36,223	4
..2	92109-630-740	IC-MOS	74ACT74 ,SOP-14		U30,206,221	3
..2	92109-631-751	IC-MOS	74ACT175 ,SOP-16		U26	1
..2	92109-632-444	IC-MOS	74ACT244 ,SOP-20	01	U10,15,218,220	
				02	U222,226,233,234	
					* Total Qty ===>	8
..2	92109-632-450	IC-MOS	74ACT245 ,SOP-20	01	U11,14,219,224	
				02	U225,227,228,504	
					* Total Qty ===>	8
..2	92109-633-730	IC-MOS	74ACT373 ,SOP-20		U12	1
..2	92109-840-662	IC-MOS	74HC4066 ,SOP-20		U24	1
..2	92109-911-284	IC-CUSTOM	WD90C61 ,PLCC-20		U9	1
..2	92111-002-410	IC-INTERFACE	MAX241 ,SOP-W28		U38	1

LEVEL	PART NUMBER	DESCRIPTION	SPECIFICATION	CC	REF-DESN	QTY
..2	92113-212-881	IC-EPROM	27C010 ,128K*8		U23	1
..2	92113-464-010	IC-DRAM	44C1000 ,1Mx4		U1-8	8
..2	92113-464-160	IC-DRAM	41664 ,64K*16		U231,232	2
..2	92113-564-081	IC-SRAM	5C6408 ,8K*8		U17,18	2
..2	92113-685-021	IC-PAL	N85C224-80		U28	1
..2	92115-180-390	IC-CPU	80386SL-20,PQFP-196		U13	1
..2	92115-187-420	IC-CPU	8742AH ,PLCC-44		U33	1
..2	92115-521-041	IC-CUSTOM	KU82360SL ,PQFP-196		U32	1
..2	92115-521-042	IC-CUSTOM	N82077SL ,PLCC		U207	1
..2	92115-549-020	IC-CUSTOM	TPC1010A ,PLCC-68		U230	1
..2	92115-561-101	IC-CUSTOM	WD90C20-LR,PQFP-132		U229	1
..2	92119-201-051	IC-LINEAR	TL7705A ,SOP-8		U37	1
..2	92119-201-180	IC-LINEAR	LM358 ,SOP-8		U501	1
..2	92119-203-850	IC-LINEAR	LM385 ,SOP-8		D3	1
..2	92119-603-240	IC-LINEAR	LM324 ,SOP-14		U29	1
..2	92119-610-200	IC-LINEAR	LT1020 ,SOP-10		U31	1
..2	92139-222-220	TR-GENERAL	MMBT2222A ,SOT-23,1B		Q203	1
..2	92139-239-041	TR-GENERAL	MMBT3904 ,SOT-23,1A		Q201,204,205	3
..2	92139-239-061	TR-GENERAL	MMBT3906 ,SOT-23,2A		Q202	1
..2	92139-510-050	FET	SMD10P05 ,SOT-23,SW		U203	1
..2	92139-599-520	FET	SI9952DY ,SOT ,SW		U39,U213	2
..2	92139-599-530	FET	SI9953DY ,SOT ,SW		U41,212,214,503	4
..2	92139-900-710	FET	2N7002LT1 ,SOT		U201,202,U502	3
..2	92169-200-130	DIODE-RECTIFIER	SS-13 ,SMD		D501	1
..2	92169-341-483	DIODE-SWITCHING	FDS04148-S		D4-6,201-206	9
..2	92169-610-041	IC-LINEAR	LT1004CS8 ,SOP		U34	1
..2	92220-158-171	DIODE-SCHOTTKY	1N5817 ,DO ,RE		D7	1
..2	92220-241-200	DIODE-SCHOTTKY	SGL41-20 ,SMD ,RE		D1,2,10,11,500	7
..2	93004-102-001	PWB	NP1-MAIN001PCB			1
..2	93310-029-050	CONN-HEADER	BM4W-THD ,5P ,1R		SJ1	1
..2	93310-030-020	CONN-HEADER	BM4W-THD ,2P ,1R		BA1	1
..2	93312-116-090	CONN-DSUB	BMP-THD ,9P ,2R		CN7	1
..2	93312-117-150	CONN-DSUB	BMR-THD ,15P ,2R		CN3	1
..2	93312-117-250	CONN-DSUB	BMR-THD ,25P ,2R		CN4	1
..2	93345-007-140	CONN-SOCKET	HDR-THD ,14P ,1R		JP2,2	2
..2	93345-008-600	CONN-C/E	BMR-THD ,68P ,4R		CN201	1
..2	93345-017-260	CONN-DSUB	BMR-THD ,26P ,4R		CN6	1
..2	93345-037-100	CONN-SOCKET	HDR-THD ,10P ,1R		JP1,JP3	2
..2	93345-051-002	CONN-JACK	DIN-THD ,6P		CN9	1
..2	93345-073-020	CONN-HEADER	BM4W-THD ,2P ,1R		JP5	1
..2	93345-108-100	CONN-SOCKET	FFC-SMD ,20P ,1R		CN1	1
..2	93345-108-500	CONN-C/E	BMR-SMD ,50P ,2R		CN5	1

LEVEL	PART NUMBER	DESCRIPTION	SPECIFICATION	CC	REF-DESN	QTY
..2	93345-128-140	CONN-SOCKET	HDR-SMD ,14P ,2R		CN8	1
..2	93345-129-020	CONN-HEADER	BM4W-THD ,2P ,1R		JP5	1
..2	93345-308-300	CONN-SOCKET	SMD ,30P		CN2	1
..2	93345-308-600	CONN-C/E	BMR-SMD ,60P ,2R		SJ2	1
..2	93354-232-001	SOCKET-IC	PLCC-SMD ,32P ,2R		U23	1
..2	93354-268-001	SOCKET-IC	PLCC-SMD ,68P ,2R		U27	1
..2	94049-903-960	CORE-FERRITE	HF50ACB322513-T(TDK)	01	L1,3-12,500	
				02	L201-209,211-220	
					* Total Qty ===>	31
..2	94209-902-040	SPEAKER	MG-25 (TRASDUCE)		LS1	1
..2	94529-210-201	FILTER	ACF451832-102T(TDK)	01	LC201,202,512	
				02	LC513	
					* Total Qty ===>	4
..2	94529-470-200	FILTER	ACF451822-470(TDK)	01	LC203-207	
..2	94529-470-200	FILTER	ACF451822-470(TDK)	02	LC500-511	
					* Total Qty ===>	17
..2	94538-014-311	CRYSTAL(SMD)	14.31818M ,50PPM ,SM		CR201	1
..2	94538-024-001	CRYSTAL(SMD)	24 MHZ ,50PPM ,SM		CR202	1
..2	94538-032-760	CRYSTAL(SMD)	32.768 KHZ,30PPM ,SM		CR1	1
..2	94539-016-005	CRYSTAL	16 MHZ ,100PPM,TH		1OSC	1
..2	94539-040-003	CRYSTAL	40 MHZ ,100PPM,TH		2OSC	1
..2	94539-903-110	CRYSTAL	1.8432 MHZ,50PPM ,HC		3OSC	1
..2	94709-902-710	FUSE	251004 (LITTEL)		F1,F2	2
..2	94709-903-220	FUSE	251.500 (LITTLE)		F201	1
..2	94719-901-312	BATTERY	TL5186 (TADIRAN)		BT1	1
..2	96612-923-510	BRACKET	B/K CONN. ,SUS 0.15t			1
..2	96673-901-010	SPRING	BATT.-CONT,BECU C172		BC1-4	4
..2	98114-375-001	LABEL-IC	KBD BIOS,N386S/25			1
..2	98114-375-005	LABEL-IC	ROM BIOS,N386/25			1
..2	98114-375-049	LABEL-IC	PCMCIA,13*12MM,NOTEP			1
..2	98114-375-051	LABEL-IC	PAL,10*7MM,NOTEPAD1			1
.1	99112-102-811	ASS'Y LCD CTRL B'D	NOTEPAD1 LCD CTRL B'D			1
..2	91083-102-750	R-CARBON CHIP	1K ,5% ,1/10W ,C		R5	1
..2	91083-103-750	R-CARBON CHIP	10K ,5% ,1/10W ,C		R6	1
..2	91083-122-710	R-CARBON CHIP	1.2K ,1% ,1/10W ,C		R3	1
..2	91083-203-750	R-CARBON CHIP	20K ,5% ,1/10W ,C		R4	1
..2	91083-331-750	R-CARBON CHIP	330 ,5% ,1/10W ,C		R1,2	2
..2	91212-203-841	VR-SLIDE	20K ,20% ,1/40W ,R		VR1,VR2	2
..2	91301-104-310	C-CERAMIC CHIP	0.1uF ,10% ,50V ,X		C1-4,C11	5
..2	91629-106-530	C-TANTAL CHIP	10uF ,10% ,50V ,G		C7	1
..2	91629-106-640	C-TANTAL CHIP	10uF ,10% ,16V ,G		C5,6	2
..2	92309-310-001	LED	CL-150PG-CD-T		D2,3	2
..2	92309-330-000	LED	CL-150Y-CD-T		D4	1

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..2	93004-102-802	PWB	NP1-CTRL002PCB			1
..2	93310-029-140	CONN-HEADER	BM4W-THD ,14P ,1R		JP1	1
..2	93510-050-013	SWITCH-SLIDE	SKHHAL h=4mm		SR1	1
..2	93510-314-020	SWITCH-SLIDE	SSSS922(G9539653M)		SW1	1
.1	99112-102-812	ASS'Y DIGIT CTRL B'D	NOTEPAD1 DIGIT CTRL			1
..2	91083-101-751	R-CARBON CHIP	100 ,5% ,1/10W ,C		R20-22	3
..2	91083-102-750	R-CARBON CHIP	1K ,5% ,1/10W ,C		R19	1
..2	91083-103-750	R-CARBON CHIP	10K ,5% ,1/10W ,C		R18	1
..2	91083-104-750	R-CARBON CHIP	100K ,5% ,1/10W ,C		R31	1
..2	91083-105-710	R-CARBON CHIP	1M ,1% ,1/10 ,C		R1	1
..2	91083-183-710	R-CARBON CHIP	18K ,1% ,1/10W ,C		R10-13	4
..2	91083-220-710	R-CARBON CHIP	22 ,1% ,1/10W ,C		R9	1
..2	91083-221-710	R-CARBON CHIP	220 ,1% ,1/10W ,C		R23,24	2
..2	91083-222-710	R-CARBON CHIP	2.2K ,1% ,1/10W ,C		R5	1
..2	91083-273-750	R-CARBON CHIP	27K ,5% ,1/10W ,C		R4	1
..2	91083-302-750	R-CARBON CHIP	3K ,5% ,1/10W ,C		R14	1
..2	91083-362-710	R-CARBON CHIP	3.57K ,1% ,1/10 ,S		R3	1
..2	91083-390-750	R-CARBON CHIP	39 ,5% ,1/10W ,C		R15,16	2
..2	91083-472-750	R-CARBON CHIP	4.7K ,5% ,1/10W ,C		R30,32	2
..2	91083-473-750	R-CARBON CHIP	47K ,5% ,1/10W ,C		R6	1
..2	91083-479-750	R-CARBON CHIP	4.7 ,5% ,1/10W ,S		R7,8,25-29,33	8
..2	91083-820-750	R-CARBON CHIP	82 ,5% ,1/10W ,C		R17	1
..2	91083-832-710	R-CARBON CHIP	8.25K ,1% ,1/10W ,C		R2	1
..2	91302-104-120	C-CERAMIC CHIP	0.1uF ,Z	01	C1,2,5,11	
				02	C12,14,16	
					* Total Qty ===>	7
..2	91302-331-750	C-CERAMIC CHIP	330pF ,50V ,Z		C18	1
..2	91302-390-750	C-CERAMIC CHIP	39pF ,5% ,50V		C6,7	2
..2	91302-474-160	C-CERAMIC CHIP	0.47uF,+80 ,16V		C8,10	2
..2	91302-475-160	C-CERAMIC CHIP	4.7uF ,+80 ,16V ,Z	01	C19-24,3,4,9	
				02	9,13,15,17	
					* Total Qty ===>	12
..2	92113-264-161	IC-EEPROM	93C46 ,64*16		IC5	1
..2	92115-562-010	IC-CUSTOM	W5000F ,PQFP		IC2	1
..2	92115-562-020	IC-CUSTOM	W37700XX ,PQFP		IC1	1
..2	92115-562-030	IC-CUSTOM	W6001 ,PQFP		IC3	1
..2	92115-562-040	IC-CUSTOM	W6002 ,PQFP		IC4	1
..2	92410-321-050	INDUCTOR	BLM21A05PT (MURATA)		L1-3	3
..2	93004-102-801	PWB	NP1-DGT001PCB			1
..2	93345-022-140	CONN-HEADER	BMNW-THD ,14P ,1R		CN2,3	2

LEVEL	PART NUMBER	DESCRIPTION	SPECIFICATION	CC	REF-DESN	QTY
..2	93345-312-300	CONN-SOCKET	SMD ,30P ,1R		CN1	1
..2	94538-016-002	CRYSTAL	16 MHZ ,30PPM ,SM		X1	1
.1	99112-102-830	ASSY-PEN GRY	STYLUS PEN 2 S/W			1
..2	94992-100-003	STYLUS-PEN	UP-201-04A (WACOM)			1
.1	99112-102-851	ASSY FAX-MODEM B'D	NOTEPAD1 F-MODEM ,SE			1
..2	93042-450-050	BOARD-ASSY	CH1789S (CERMETEK)			1
..2	93053-408-120	CABLE-INTERFACE	MODEM,7 FEET 50M			1
..2	98134-375-045	MANUAL-USERS GUIDE	FAX/MODEM,SAMSUNG			1
.1	99112-102-SUB	ASSY-SUBMATERIAL	NOTEPAD1			1
..2	90469-100-008	SOLDER-WIRE	SN63 PB37 3.0W WATER			0
..2	90469-120-210	SOLDER-BAR	S63S-BAR WATER			0
..2	90469-130-010	SOLDER	SOLDER PASTE/WS601 S			0
..2	90469-130-020	SOLDER	SOLDER WIRE OA 0.5MM			0
..2	90469-130-030	SOLDER	SOLDER WIRE OA 1.27M			0
..2	90469-130-040	SOLDER	SOLDER WIRE OA 1.0 S			0
..2	90469-200-230	SOLDER	1.0mm,Sn60/Pb40,KR-1			0
..2	90479-100-010	FLUX	NF-3000			0
..2	90809-100-041	ADHESIVE-SMT	PD860002S/SP(HERAEUS			0
..2	90849-110-010	THINNER	UL-1000			0
..2	94099-000-020	DISKETTE-BLANK	3.5",M-2HD			0
.1	99114-102-801	ASS'Y-HARNESS	NOTE PAD1			1
..2	93056-102-001	HARNESS-ASSY	INVERTER CBL,NOTEPAD			1
..2	93056-102-002	HARNESS-ASSY	HDD FPC CBL,NOTEPAD1			1
..2	93056-102-003	HARNESS-ASSY	CTRL BD CBL,NOTEPAD1			1
..2	93120-102-810	CABLE-FLAT/FFC	20P,40M,1MM			1
.1	99114-102-810	ASS'Y LCD/DIGITIZER	NOTEPAD1 LCD/DIGITIZ			1
..2	94985-102-810	LCD-PANEL	H6481L-FF (CITIZEN)			1
.1	99114-102-831	ASSY-BATTERY	NOTEPAD1 AUX BATT PA			1
..2	94719-102-820	BATTERY	6N-50AAA (SANYO)			1
.1	99114-102-832	ASSY-BATTERY (SEC)	NOTEPAD1 MAIN BATT,S			1
..2	94719-102-800	BATTERY-PACK	10KR-1700AE,GRID			1
...3	92189-900-920	THERMISTOR	103AT-2			1
...3	94719-102-810	BATTERY-PACK	10KR-1700AE (SANYO)			1
..2	98114-375-063	LABEL-ETC	WARNING BATTERY,SEC			1
..2	98114-375-064	LABEL-ETC	DATE-CODE,BATTERY			1
.1	99115-102-020	ASSY-PACKING (SEC)	NOTEPAD1			1
..2	90899-100-013	DRY-GEL	DESICCANT M-2 20GR			2
..2	96001-977-510	CARRYING CASE	PROTECTIVE,ABS+LEATH			1
..2	97663-900-410	HANDLE-PACKING	P.E,WHITE			1
..2	97663-900-510	HANDLE-PAD	P.E,WHITE			1
..2	98114-372-007	LABEL-BARCODE	BOX,110*70MM,ALL MOD			2
..2	98613-920-420	PACKING CASE	BOX ,SW4-B LAM			1

LEVEL	PART NUMBER	DESCRIPTION	SPECIFICATION	CC	REF-DESN	QTY
..2	98654-905-310	PE BAG	,HDPE 290*			1
..2	98654-905-910	PE BAG	,HDPE 150*			2
..2	98654-906-010	PE BAG	,HDPE 100*			1
..2	98703-903-510	PAD	CUSHION ,SW1-B			1
..2	98713-904-410	CUSHION	MANUAL ,EPS			1
..2	98713-904-610	CUSHION	SYSTEM ,EPE(EPERA)			2
.1	99115-102-090	ASSY-PALLET	NOTEPAD1			1
..2	90899-900-110	PE FILM	LDPE 0.05TX2400			0
..2	98114-912-910	LABEL	PALLETE:ART PAPER 1			0
..2	98643-903-620	PALLET	PALLET ,WOODEN 12			0
..2	98654-904-730	PE-FILM	CLEANWRAP 20U X 500M			0
..2	98703-902-510	PAD	PALLETE ,CB-SW4,B,			0
..2	98704-903-020	L-PAD	K550*5 A1(250)GR YEL			0
..2	98794-202-110	AIR-BAG CONTAINER	HDPE+PAPER			0
.1	99116-102-8US	ASSY-S/W&MNL(UTILITY	NOTEPAD1,UTIL,US			1
..2	94095-375-003	UTILITY S/W	NOTEPAD UTIL 3.5 SEC			0
..2	94099-000-010	DISKETTE-BLANK	3.5",M-2DD			1
..2	98114-913-310	LABEL-DISKETTE	SYSTEM UTI,ENG,3.5",			1
.1	99116-50A-US1	ASSY-S/W&MNL(MSDOS)	V5.0A,US,3.5",SEC			1
..2	94091-500-200	DISKETTE-S/W ASSY	MS-DOS 50A 3.5 SEC			1
.1	99116-PM3-US1	ASSY-USER'S(US VER)	NOTEPAD1 (US VER)			1
..2	98134-375-032	MANUAL-USERS GUIDE	NOTEPAD 1,ENGLISH			1
.1	99117-102-010	ASSY-MECHANICAL	NOTEPAD1			1
..2	96031-902-110	HOUSING	INTERNAL C,PC/ABS VB			1
..2	97002-120-601	SCREW-MACHINE	FH + M2.0 6.0 FZ			1
..2	97088-126-051	SCREW-BH	+2.6*5.0 FE FZY(H/T)			5
..2	97088-126-203	SCREW-MACHINE	BH + 2.6 20 FZ			4
.1	99119-102-802	ASSY-ETC (SI1)	PM386SL/20 ,SI1			1
..2	93053-861-620	POWER-CORD	PV0305CBS6F105CGSVT			1
..2	96634-900-310	BAND-RUBBER	+1.0(W) SBR W4 FD			1
.1	99122-102-863	ASSY- HDD	NOTEPAD1,QUAN(60MB)			1
..2	94971-325-060	HDD	GO DRIVE 60AT			1
..2	96612-923-010	BRACKET	HDD ,EGI			1
..2	97088-130-041	SCREW-BH	+M3*4 FE FZY(H/T)			1
.1	99123-102-841	ASS'Y DC/DC CON B'D	NOTEPAD1 DC/DC CONV			1
..2	91083-101-150	R-CARBON CHIP	100 ,5% ,1/8W ,C	1	R5	1
..2	91083-102-150	R-CARBON CHIP	1K ,5% ,1/8W ,C	1	R7,35,38,52	4
..2	91083-103-110	R-CARBON CHIP	10K ,1% ,1/8W ,C	1	R9,21,30	3
..2	91083-103-150	R-CARBON CHIP	10K ,5% ,1/8W ,C	1	R3,16,17,28,47	5
..2	91083-104-110	R-CARBON CHIP	100K ,1% ,1/8W ,C	1	R15,54	2
..2	91083-104-150	R-CARBON CHIP	100K ,5% ,1/8W ,C	1	R12,13,22,56	4
..2	91083-106-150	R-CARBON CHIP	10M ,5% ,1/8W ,C	1	R29	1
..2	91083-122-110	R-CARBON CHIP	1.2K ,1% ,1/8W ,C	1	R40,48	2

LEVEL	PART NUMBER	DESCRIPTION	SPECIFICATION	CC	REF-DESN	QTY
..2	91083-183-110	R-CARBON CHIP	18.2K ,1% ,1/8W ,C	1	R46	1
..2	91083-184-110	R-CARBON CHIP	180K ,1% ,1/8W ,C	1	R18,23,42	3
..2	91083-221-150	R-CARBON CHIP	220 ,5% ,1/8W ,C	1	R53	1
..2	91083-223-150	R-CARBON CHIP	22K ,5% ,1/8W ,C	1	R27	1
..2	91083-271-350	R-CARBON CHIP	270 ,5% ,0.5W ,C	1	R1	1
..2	91083-273-110	R-CARBON CHIP	27K ,1% ,1/8W ,C	1	R39	1
..2	91083-284-110	R-CARBON CHIP	282K ,1% ,1/8W ,C	1	R14	1
..2	91083-303-110	R-CARBON CHIP	30K ,1% ,1/8W ,C	1	R2,8,20	3
..2	91083-304-150	R-CARBON CHIP	300K ,5% ,1/8W ,C	1	R10,41,55	3
..2	91083-433-110	R-CARBON CHIP	43K ,1% ,1/8W ,C	1	R19,24,57	3
..2	91083-472-150	R-CARBON CHIP	4.7K ,5% ,1/8W ,C	1	R25,31,33,44	4
..2	91083-473-150	R-CARBON CHIP	47K ,5% ,1/8W ,C	1	R26,32,34,37,45	
				2	R50	
					* Total Qty ===>	6
..2	91083-474-150	R-CARBON CHIP	470K ,5% ,1/8W ,C	1	R36	1
..2	91083-681-150	R-CARBON CHIP	680 ,5% ,1/8W ,C	1	R51	1
..2	91083-822-150	R-CARBON CHIP	8.2K ,5% ,1/8W ,C	1	R6	1
..2	91083-823-150	R-CARBON CHIP	82K ,5% ,1/8W ,C	1	R11	1
..2	91301-103-251	C-CERAMIC CHIP	10nF ,5% ,50V ,X	1	C7,8,18	3
..2	91301-104-052	C-CERAMIC CHIP	0.1uF ,20% ,50V ,Z	1	C1,2,3,13,14	
				2	C17,20,21,22,23	
				3	C24,27,32,35,38	
				4	C39,40,42,43,44	
				5	C45,46,47,48	
					* Total Qty ===>	24
..2	91301-220-751	C-CERAMIC CHIP	22pF ,5% ,50V ,N	1	C25,26	2
..2	91301-222-351	C-CERAMIC CHIP	2200pF,10% ,50V ,X	1	C15	1
..2	91301-223-750	C-CERAMIC CHIP	22nF ,5% ,50V ,X	1	C29	1
..2	91301-473-253	C-CERAMIC CHIP	47nF ,5% ,50V ,X	1	C9	1
..2	91311-106-560	C-ELECTRONIC	10uF ,20% ,50V	1	C31	1
..2	91311-127-160	C-ELECTRONIC	120uF ,20% ,10V	1	C12	1
..2	91311-227-261	C-ELECTRONIC	220uF ,20% ,25V	1	C4	1
..2	91311-337-261	C-ELECTRONIC	330uF ,20% ,25V	1	C6	1
..2	91311-566-260	C-ELECTRONIC	56uF ,20% ,25V	1	C28	1
..2	91311-566-560	C-ELECTRONIC	56uF ,20% ,50V	1	C33,36	2
..2	91311-566-660	C-ELECTRONIC	56uF ,20% ,16V	1	C34,37	2
..2	91311-686-560	C-ELECTRONIC	68uF ,20% ,50V	1	C30	1
..2	91312-106-560	C-ELEC CHIP	10uF ,20% ,50V	1	C41	1
..2	91312-106-660	C-ELEC CHIP	10uF ,20% ,16V	1	C19	1
..2	91312-475-360	C-ELEC CHIP	4.7uF ,20% ,35V ,G	1	C16	1
..2	91602-227-161	C-ELECTRONIC	220uF ,20% ,	1	C11	1
..2	91602-337-260	C-ELECTRONIC	330uF ,20% ,25V	1	C5	1
..2	91629-475-310	C-TANTAL CHIP	4.7uF ,20% ,35V ,G	1	C10	1

LEVEL	PART NUMBER	DESCRIPTION	SPECIFICATION	CC	REF-DESN	QTY
..2	92115-587-050	IC-CUSTOM	68HC705 ,SOP-28	1	U4	1
..2	92119-201-180	IC-LINEAR	LM358 ,SOP-8	1	U5	1
..2	92119-610-720	IC-LINEAR	1072CT-F ,TO-220	1	U6	1
..2	92119-611-550	IC-LINEAR	1155CS8 ,SOP-8	1	U10	1
..2	92119-612-710	IC-LINEAR	1271CT-F ,TO-220	1	U1	1
..2	92119-614-320	IC-LINEAR	1432CS8 ,SOP-8	1	U2	1
..2	92119-629-510	IC-LINEAR	LP2951CM-X,SOT-8	1	U3	1
..2	92119-678-120	IC-LINEAR	78L12ACZ ,TO-92	1	U7	1
..2	92119-679-050	IC-LINEAR	79L05ACZ ,TO-92	1	U8	1
..2	92139-244-030	TR-GENERAL	MMBT4403L ,SOT	1	Q4,6	2
..2	92139-900-710	FET	2N7002LT1 ,SOT	1	Q1,2,3,5,8	5
..2	92169-200-130	DIODE-RECTIFIER	SS-13 ,SMD	1	D12	1
..2	92169-200-330	DIODE-RECTIFIER	SS-33 ,SMD	1	D3	1
..2	92169-210-070	DIODE-SWITCHING	RLS4148 ,SMD	1	D1,2,4,5,6,7,8	
				2	D9,10,16,17	
					* Total Qty ==>	11
..2	92169-406-481	DIODE-SWITCHING	1N4148 ,DO	1	ZD4	1
..2	92169-407-520	DIODE-ZENER	MLL752AT1 ,SMD	1	ZD2	1
..2	92179-107-030	THYRISTOR	MCR703ARL ,SMD	1	SCR1	1
..2	92211-501-550	FET	SMD15N05 ,TO-252	1	Q12	1
..2	92220-200-410	DIODE-RECTIFIER	EGL41C ,SMD	1	D13	1
..2	92220-200-415	DIODE-RECTIFIER	EGL41B ,SMD	1	D14,15	2
..2	92220-407-570	DIODE-ZENER	1N757A ,DO ,9	1	ZD1	1
..2	92220-409-670	DIODE-ZENER	1N967B ,DO ,18	1	ZD4	1
..2	92220-641-360	DIODE-VOLT SUPR	TGL41-36A ,SMD	1	ZD3	1
..2	93004-375-005	PWB	FR-4,113.8*48.8,1.2t	1	PWB	1
..2	93310-008-600	CONN-C/E	BMP-SMD ,60P ,2R	1	CN2	1
..2	93320-051-050	CONN-JACK	DIN-THD ,4P ,R/	1	CN1	1
..2	93710-106-020	INDUCTOR	10uH,DRUM 4*5.5,2.5	1	L4	1
..2	93710-150-500	INDUCTOR	005FA,OWA6,5*7.5,5uH	1	L3	1
..2	93710-506-010	INDUCTOR	MPP55050,50uH	1	L1,L2	2
..2	93730-101-010	TRANSFORMER	B50,EI1916	1	T1	1
..2	94049-903-941	CORE-FERRITE	2743019447 (F/R)	1	B1,2,3	3
..2	94049-903-960	CORE-FERRITE	HF50ACB322513-T(TDK)	1	B4	1
..2	94538-004-002	CRYSTAL	4 MHZ ,50PPM ,AT	1	X1	1
..2	94709-386-010	FUSE	251-003-T (LITTLE)	1	F1	1
..2	94709-903-020	FUSE	TR5-T NO.19374K (WM)	1	F2	1
..2	94709-903-315	FUSE-HOLDER	NO.19560(WICKMANN)	1	F2	1
..2	94729-900-732	RELAY	TQ2-2M-9V	1	RL1	1
..2	95684-970-810	HEATSINK	HEATSINK ,AL 1.5t S			1
..2	96143-900-410	SHIELD	DC/DC POWR,SPTE 0.25			1
..2	96674-906-810	FINGER-GROUND	97-520 (ISC)			1
..2	97031-126-501	SCREW-SET	+P M 2.6 5.0 ZP			1

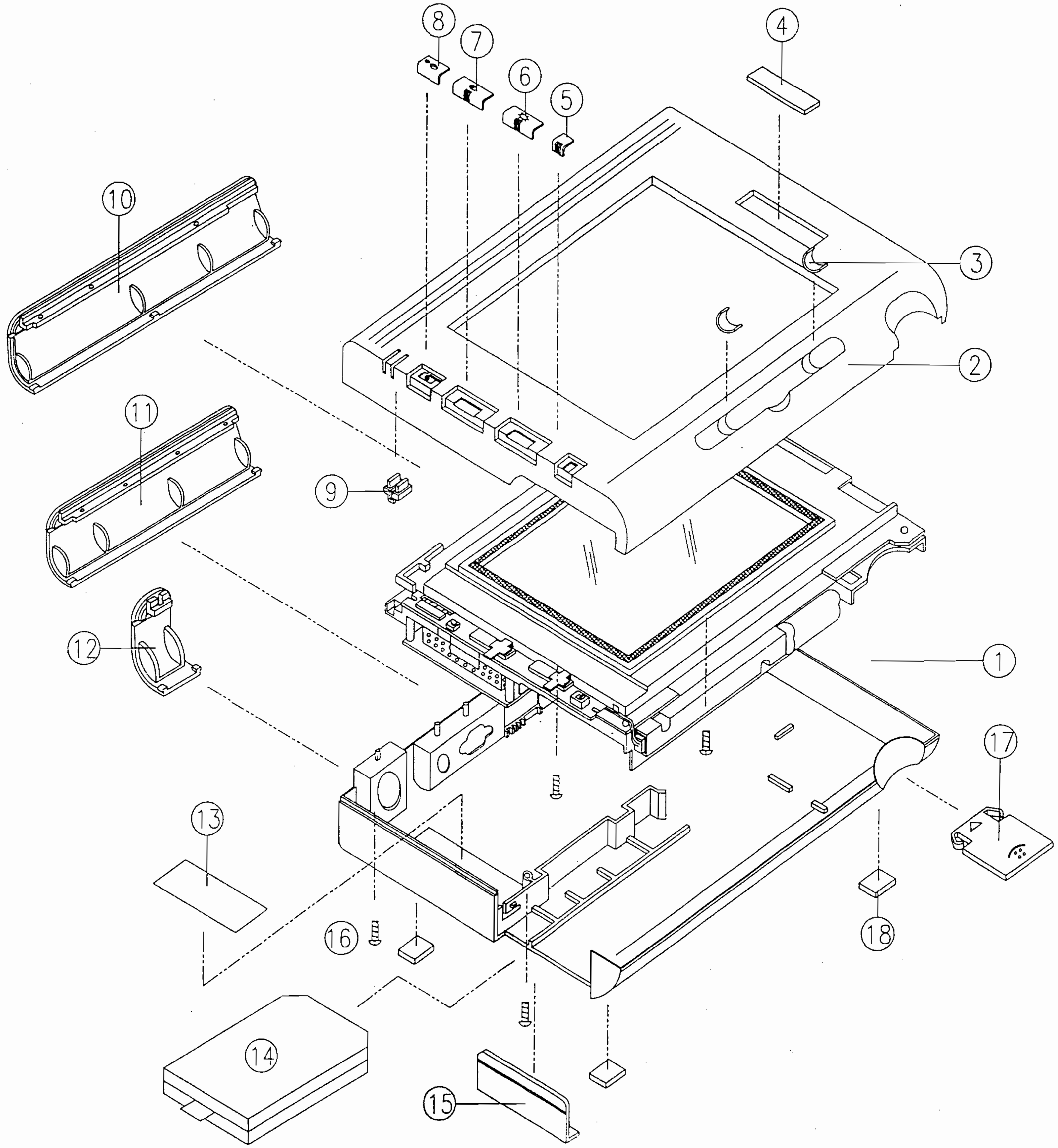
PART LIST(AC ADAPTER)

RECORD	DESCRIPT	RP SPEC	VENDOR	QTY	LOCA
1	PCB-MAIN,SUB,LED	CEM1 126*72*1.6T	CHEONGJOO	1	PCB
2	HEATSINK A	#52 AL1050P T2.5	MIKYUNG	1	HEATSINK
3	HEATSINK B	#53 AL1050P T2.5	MIKYUNG	1	HEATSINK
4	CASE-COVER	VB1108R T2.5 DARK-GRAY	KYUNGIN ENG	1	(AD-26A,C,D)
5	CASE-BOTTOM	VB1108R T2.5 DARK-GRAY	KYUNGIN ENG	1	(AD-26A,C,D)
6	CLAMP-TR(CLAMP-9)	TO-3P T1.6 ZN-W	YULIM	1	CLAMP
7	INSULATOR-SHEET	37*14*0.5T PVC	YUILL	1	INSULATOR
8	SIL-PAD	0.3T SILICON AR230	APEX	2	INSULATOR
9	SIL-PAD CAP	0.39T SILICON AR1720	APEX	1	INSULATOR
10	LED-HOLDER:ACRYL	44*5.5*8.5T NATURAL	SINILL	1	LED-HOLDER
11	SCREW-M	FH+ M3*10	YULIM	2	SCREW-M
12	SCREW-M	FH+ M3*12	YULIM	1	SCREW-M
13	SCREW-P	FH+ M3*25	YULIM	4	SCREW-P
14	SCREW-P	PH+ M3*8	YULIM	1	SCREW-P
15	SCREW-P	RH+ M3*8	YULIM	2	SCREW-P
16	NUT-HEX	M3*2.2	YULIM	2	NET-HEX
17	WASHER-SPRING	I3*R5.9*T0.7		2	D8,Q4
18	SPACER	I3.2 R8*4.5 L6 NYLON66		1	D8
19	FOOT	10*10*1.6T BLACK SJ5816	DAEYUNG,YUILL	4	FOOT
20	TR-PNP TO-92	2N3906 -40V 200MA 0.6W	SEC,MOTO	1	Q2
21	TR-PNP TO-126	KSB1151-Y-60V 5A 20W	SEC	1	Q4
22	TR-NPN TO-92	2N3904 60V 200MA 0.6W	SEC,MOTO	1	Q3
23	FET-N TO-3P	2SK1342 900V 8A	HITACHI	1	Q1
24	FET-N MTO-3P R1	2SK1537 900V 5A 100W	SHINDENGEN	1	Q1
25	FET-N TO-92	VN2222LL 60V 150MA 0.4W	MOTO,SGS	3	Q5.6.7
26	D-BRIDGE	2KBP06M,600V 2A	G.I	1	D1
27	D-SCHOTTKY TO-220	MBR20100CT 100V 20A	MOTO,GI	1	D8
28	D-SWICHING	1N4148	TFK,KEC	2	D7,10
29	D-F RECOVERY	UF4007 1000V 1A	GI,MOTO	2	D2,3
30	D-SCHOTTY DO-201AD	1N5822 40V 3A	G.I,MOTO	1	D12
31	D-SCHOTTY DO-201 R1	D3S4M 40V 3A	SHINDENGEN	1	D12
32	D-ZENER	1N5223B 2.7V 0.5W	MOT,ST	1	D11
33	D-ZENER	1N5239B 9.1V 0.5W	MOT,ST	1	D6
34	D-ZENER	1N5245B 15V 0.5W	MOT,ST	2	D4.5
35	D-ZENER	1N5250B 20V 0.5W	MOT,ST	1	D9
36	R-CARBON	100 J 1/8W	HANJOO	1	R29
37	R-CARBON	1K J 1/8W	HANJOO	1	R9
38	R-CARBON	1K J 1/2W	HANJOO	1	R24
39	R-CARBON	10K J 1/2W	HANJOO	3	R18,26,36

RECORD	DESCRIPT	RP SPEC	VENDOR	QTY	LOCA
40	R-CARBON	100K J 1/8W	HANJOO	2	R28,42
41	R-CARBON	1.2K J 1/8W	HANJOO	1	R21
42	R-CARBON	12K J 1/8W	HANJOO	1	R8
43	R-CARBON	13K J 1/8W	HANJOO	1	R41
44	R-CARBON	1.5K J 1/8W	HANJOO	1	R16
45	R-CARBON	180 J 1/8W	HANJOO	1	R7
46	R-CARBON	200 J 1/8W	HANJOO	1	R12
47	R-CARBON	300 J 1/8W	HANJOO	1	R11
48	R-CARBON	2.2K J 1/4W	HANJOO	1	R30
49	R-CARBON	24K J 1/8W	HANJOO	1	R10
50	R-CARBON	30 J 1/4W	HANJOO	1	R6
51	R-CARBON	300 J 1/2W	HANJOO	1	R5
52	R-CARBON	33K J 1/8W	HANJOO	1	R35
53	R-CARBON	3.9K J 1/4W	HANJOO	2	R23,25
54	R-CARBON	47 J 1/4W	HANJOO	1	R4
55	R-CARBON	47 J 1/2W	HANJOO	1	R14
56	R-CARBON	4.7K J 1/8W	HANJOO	1	R19
57	R-CARBON	470K J 1/2W	HANJOO	2	R1.2
58	R-CARBON	510 J 1/8W	HANJOO	1	R17
59	R-CARBON	560 J 1/8W	HANJOO	1	R34
60	R-CARBON	5.6K J 1/8W	HANJOO	1	R22
61	R-CARBON	6.8K J 1/8W	HANJOO	3	R31.32.33
62	R-CARBON	9.1K J 1/8W	HANJOO	1	R20
63	R-METAL FILM	20K F 1/8W	PHILIPS	2	R38,40
64	R-METAL FILM	30K F 1/8W	PHILIPS	1	R39
65	R-METAL FILM	36K F 1/8W	PHILIPS	1	R37
66	R-METAL FILM	82K F 1/8W	PHILIPS	1	R43
67	R-METAL OXIDE	1K J 1W	YUMI	1	R27
68	R-METAL OXIDE	47K J 3W	YUMI	1	R3
69	R-W WOUND(N)	1 F 1W	DALE-KOREA	1	R13
70	R-W WOUND(N)	0.1 F 1W	DALE-KOREA	1	R15
71	VR-SEMI	500 10% 1/2W CT-6P	COPAL	1	VR1
72	VR-SEMI	R1 500 10% 1/2W	BURNS	1	VR1
73	VR-SEMI	2K 20% 1/2W CT-6X	COPAL	1	VR2
74	VR-SEMI	R1 2K 20% 1/2W	BURNS	1	VR2
75	CAP-C DS	102 1KV	SEMCO	2	C6,13
76	CAP-C DS	104 50V	SEMCO	1	C20
77	CAP-C DS	222 250VAC AA	SEMCO	1	C7
78	CAP-C DS	222 1KV	SEMCO	1	C23

RECORD	DESCRIPT	RP SPEC	VENDOR	QTY	LOCA
79	CAP-C DS	332 250VAC AA	SEMCO	2	C3,4
80	CAP-C DS	472 1KV	SEMCO	1	C22
81	CAP-C DS	103 50V	SEMCO	4	C11,12,17,18
82	CAP-F PET	472 100V	SEOJIN	1	C9
83	CAP-F MPET	104 250VAC KNB1350	ISKRA	1	C2
84	CAP-F MPET	224 250VAC KNB1530	ISKRA	1	C1
85	CAP-E AD	100UF 400V SMU25*30	SEMCO	1	C5
86	CAP-E AD	1UF 50V SSE 3*5	SEMCO	2	C16,21
87	CAP-E AD	10UF 50V GLT5*11	SEMCO	2	C8,10
88	CAP-E AD	1000UF 35V SXE12.5*30	SAMYOUNG	1	C14
89	CAP-E AD R1	100UF 35V STL12.5*30	SEMCO	1	C14
90	CAP-E AD	470UF 25V SXE10*20	SAMYOUNG	2	C15,19
91	CAP-E AD R1	470UF 25V STL10*20	SEMCO	2	C15,19
92	SCR,TO-220	TYN058 50V 5A	SGS	1	SCR1
93	IC-OP AMP	LM358N DIP 8PIN	SEC	1	IC3
94	IC-SHUNT REGULATOR	KA431CZ TO-92	SEC	1	IC2
95	IC-SHUNT REGULATOR	TL431 TO-92	MOTO	1	IC2
96	TRANS-SWG	PQ2625 1.1mH AD-26T1	NAMYANG	1	T1
97	CHOCK-COIL	BAR 6uH	NAMYANG	1	L1
98	LINE-FILTER	GP-9 50mH 150T	NAMYANG	1	LF1
99	LED-SQUARE	SEL4825D AMBER 2*4*5	SANKEN	2	LD2,3
100	LED-SQUARE	SEL4425G GREEN 2*4*5	SANKEN	1	LD1
101	OPTO-COUPLER	CQY80NG DIP-6PIN	TELEFUNKEN	1	IC1
102	THERMISTOR	8-OHM 3A 10SP008M	U.E.I	1	TH1
103	THERMISROR R1	8-OHM 2.6A 8D-11	ISHUKA	1	TH1
104	VARISTOR	D61ZOV301RA45 425-518V	MAIDA	1	Z1
105	CONN-INTCONN	AW-0500-05 SR 2.0 WHT	KYUNGSUNG	1	CON2
106	CONN-INTCONN	FAU-0640-09 WHT 9PIN	KYUNGSUNG	1	CON3
107	WIRE-SAHDW	D0.6 SIL(T-T)	SAMEON		JUMP
108	WIRE-SPJW	JUMP(TEFLON TUBE) D0.6	SAMEUN	1	J1
109	FUSE-SLOW BLOW	52S-020-H 250V 2A	TRIAD	1	F1(AD-26A,A1)
110	MAGENT-FRIT CORE	ZJ-41306-TC TOROIDAL	MAGETICS	1	L3
111	MAGNET-FRIT CORE	2643000101 BEAD	FAIR-RITE	3	BD1,2,3
112	ASS'Y-CONN,HOUS,OTH	5PIN 5P*90 UL1007 #28	KYUNGSUNG	1	CON1
113	ASS'Y-RECEPTACLE	0711-PN ASS'Y	KYUNGSUNG	1	HARNESS-ASS'Y
114	RECEPTALCE-ACIN&PWR	0711-PN 10A 250V	INALWAYS	1	INLET
115	MAGNET-FRIT CORE	ZJ-41306-TC TOROIDAL	MAGNECTIS	1	L2
116	ASS'Y-JACK	MDP-402-4PCA-207(AD-26)	SINGATRON	1	OUTPUT CABLE
117	TUBE-SHRINKAGE	I3.5 T0.25 2.5KV	SAMEON		OUTPUT CABLE

RECORD	DESCRIPT	RP SPEC	VENDOR	QTY	LOCA
118	TUBE-SHRINKAGE	I7.0 T0.25 2.5KV	SAMEON		FUSE(F1)
119	TUBE-PTFE	TEFLON-TUBE, I1.0, L20	SAMEON		R3
120	LABEL-RATING	SILVER PET 54*40 AD-26A	SAMKWANG	1	LABEL(AD-26A)
121	LABEL-SERIAL	PET T0.05, NOTE-PAD(MMSY)	SAMKWANG	1	LABEL(AD-26A)
122	LABEL-SERIAL	PET T0.05 UPS001001	SAMKWANG	1	LABEL(AD-26A)
123	LABEL-CAUTION	POLYSTER 36*15	SAMKWANG	1	LABEL
124	LABEL-WARNING	POLYSTER 26*17	SAMKWANG	1	LABEL
125	LABEL-GENERAL	PET T0.05 BOTTOM, YELLOW	SAMKWANG	1	OUTPUT CABLE



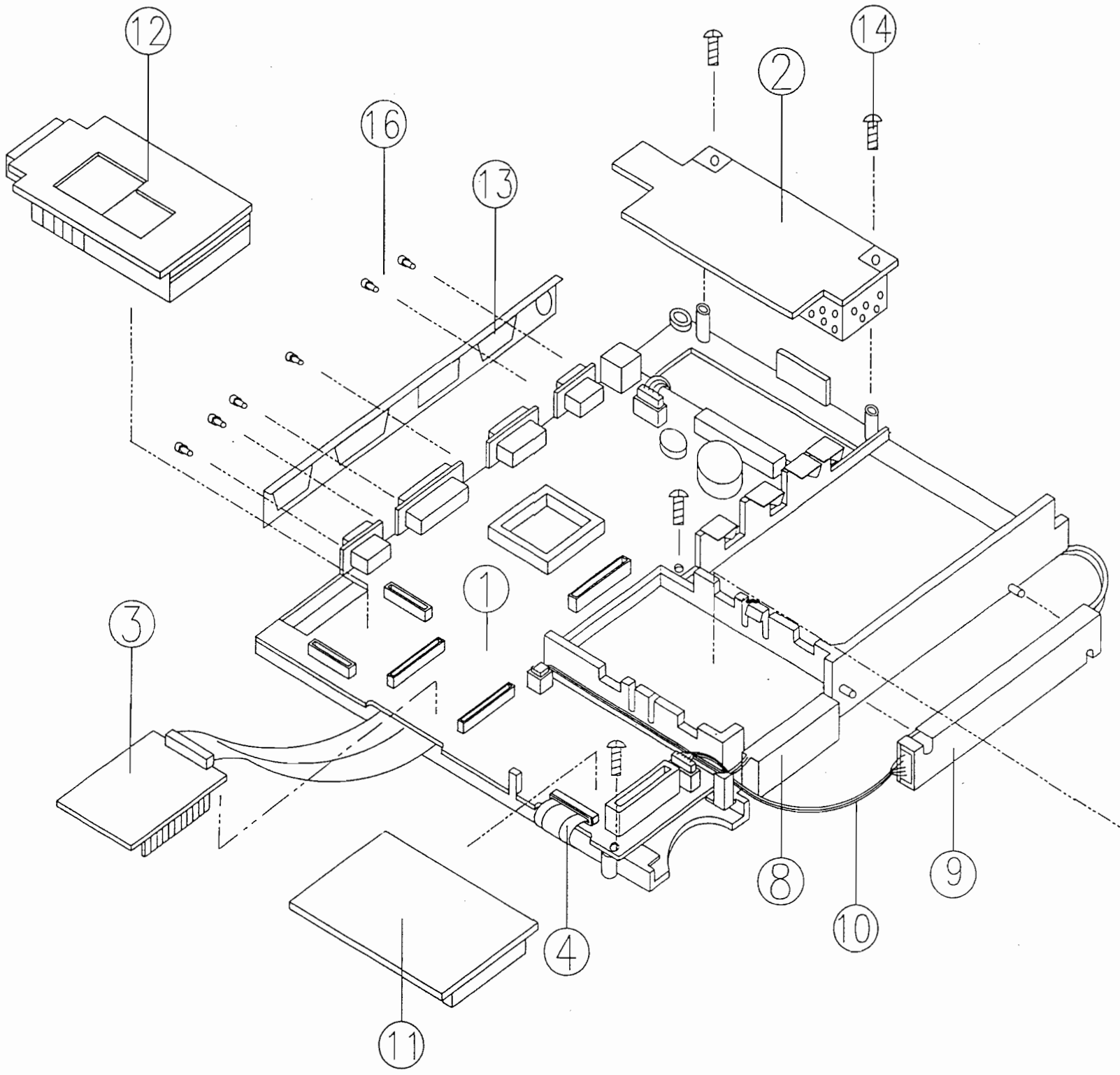
PARTS LIST

NO	DESCRIPTION	CODE - NO.	SPECIFICATION	Q'TY	REMARK
1	HOUSING BOTTOM	96031-902-010	PC/ABS	-1-	
2	HOUSING TOP	96031-901-910	PC/ABS	-1-	
3	HOLDER PEN	96602-900-710	S1550	-2-	
4	LOGO BADGE	97694-900-010	COPPER T=0.3	-1-	
5	KNOB POWER	97621-900-010	PC/ABS	-1-	
6	KNOB BRIGHTNESS	97621-900-310	PC/ABS	-1-	
7	KNOB CONTRAST	97621-900-110	PC/ABS	-1-	
8	KNOB SUS/RES'D	97621-900-210	PC/ABS	-1-	
9	LED LENS	97652-900-110	ACRYL	-1-	
10	DOOR LEFT I/O	97641-900-220	S1550	-1-	
11	DOOR RIGHT I/O	97641-900-310	S1550	-1-	
12	DOOR POWER JACK	97641-900-410	S1550	-1-	
13	INSULATOR	95904-903-010	PVC SHEET T=0.3	-1-	
14	BATTERY	99114-102-832	ASS'Y	-1-	
15	BATTERY DOOR	97641-900-110	PC/ABS	-1-	
16	SCREW	97008-126-203	BH+ M2.6 * 20 FE FZB	-4-	
17	DUMMY IC CARD	96052-904-710	PC/ABS	-1-	
18	FOOT RUBBER	98464-907-810	NEOPRENE	-4-	

REVZ. : 1992.07.02.(OHK)

EXPLODED VIEW (3/3)
NOTE-PAD

삼성전자주식회사



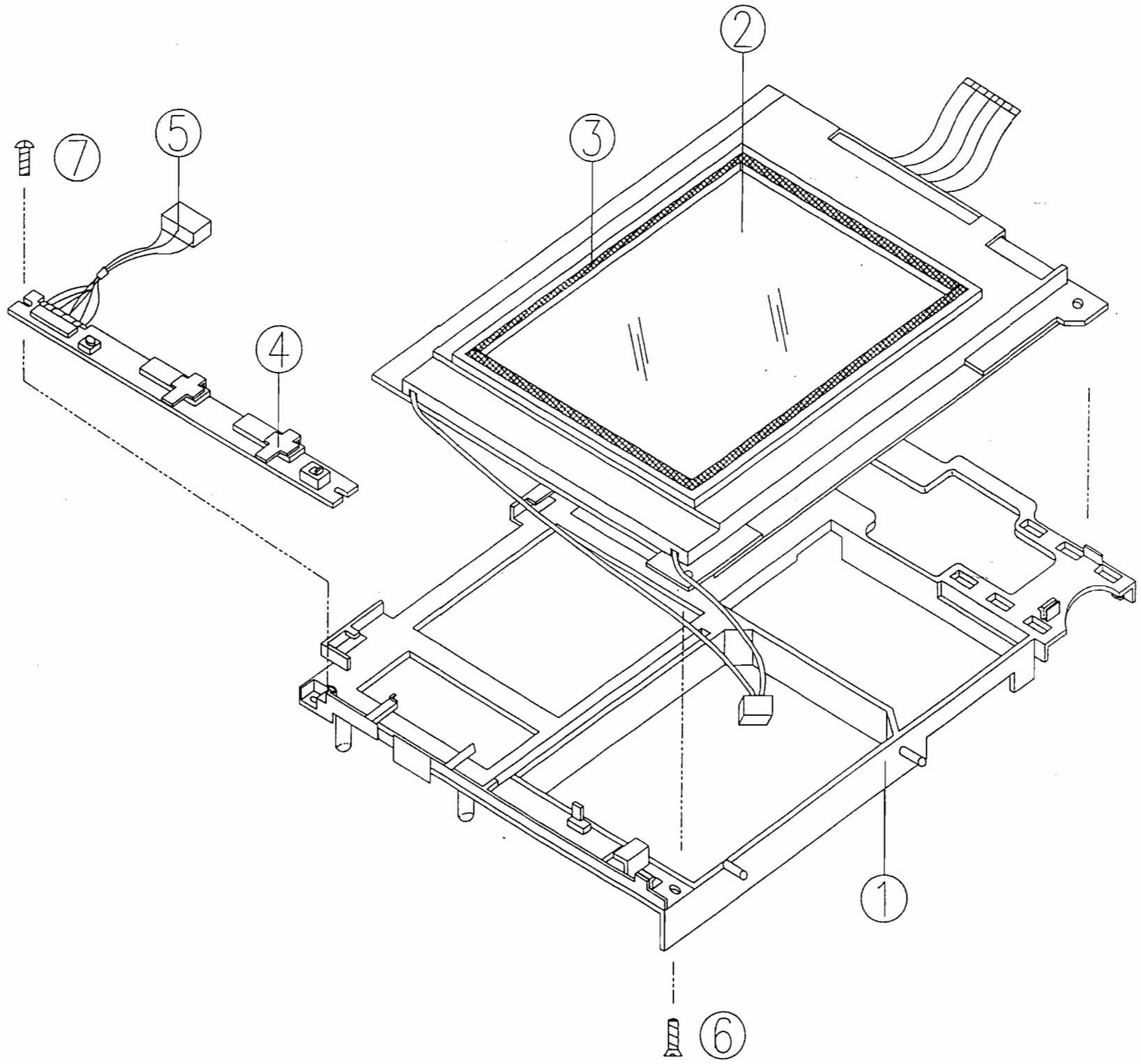
PARTS LIST

NO	DESCRIPTION	CODE - NO.	SPECIFICATION	Q'TY	REMARK
1	ASS'Y MOTHER B'D	99112-102-801		-1-	
2	ASS'Y DC/DC CONV B'D	99123-102-841		-1-	
3	ASS'Y DIGIT CTRL B'D	99112-102-812		-1-	
4	LCD CABLE	93120-102-810		-1-	
5	HDD	94971-325-060	60MB, QUANTUM	-1-	
6	HDD BRACKET	96612-923-010	E.G.I T=0.5	-1-	
7	HDD FPC	93056-102-002		-1-	
8	BRIDGE BATERRY	94719-901-312		-1-	
9	ASS'Y DC/AC INV B'D	94914-140-020		-1-	
10	INVERTER HARNESS	93056-102-001		-1-	
11	MEMORY CARD ASS'Y	99112-102-820		-1-	
12	ASS'Y MODEM B'D	93042-450-050		-1-	
13	BRACKET CONNECTOR	96612-923-510	STS T=0.15	-1-	
14	SCREW	97008-126-051	BH+ M2.6+5 FE FZY	-4-	
15	SCREW	97063-130-041	BH+ M3.0+4 FE FZY	-4-	
16	SCREW HEX	INPUT WITH CONNECTOR ASS'Y		-6-	

REV2. : 1992.07.02.(OHK)

EXPLODED VIEW (2/3)
NOTE-PAD

삼성전자주식회사



PARTS LIST

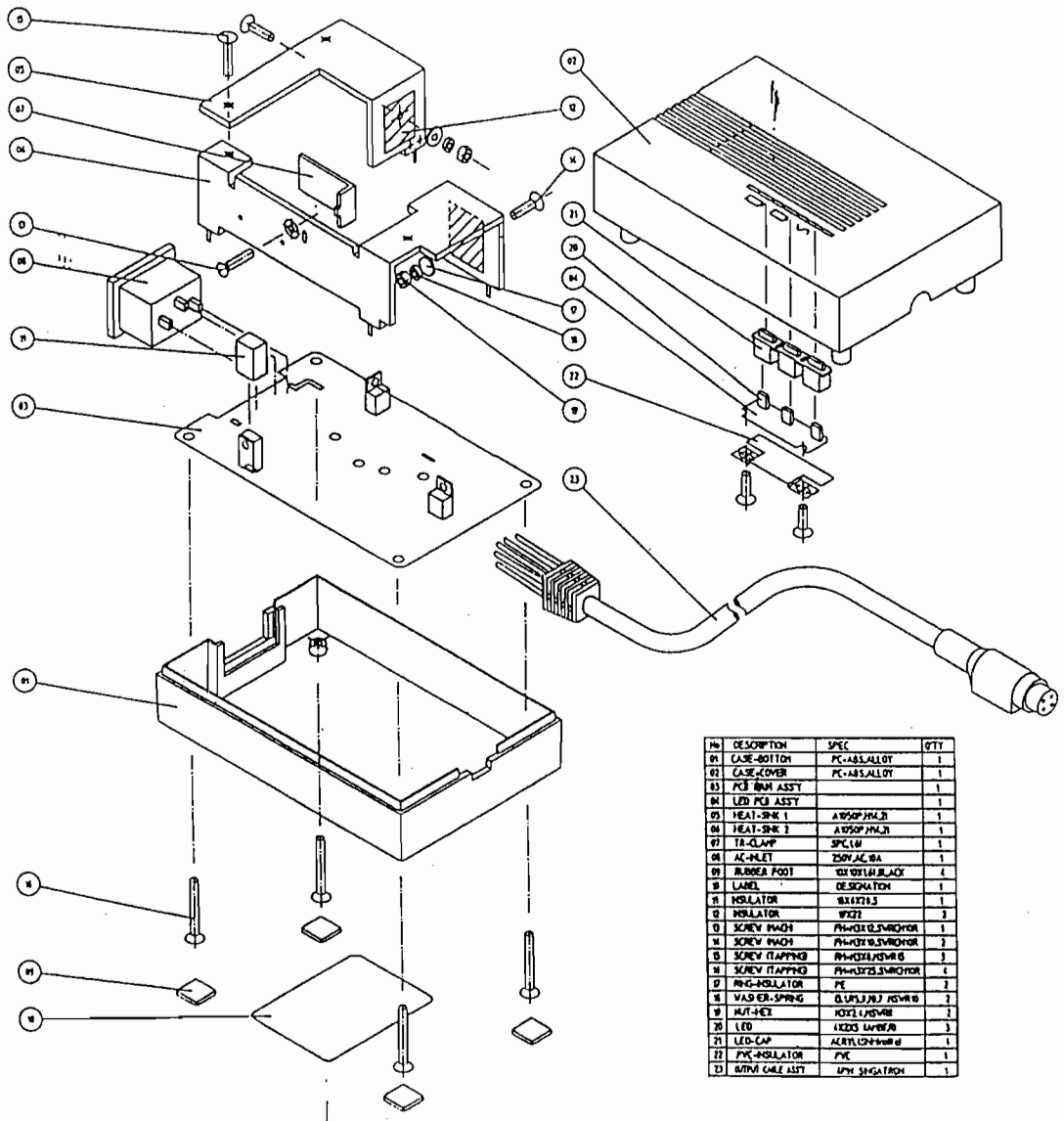
NO	DESCRIPTION	CODE - NO.	SPECIFICATION	Q'TY	REMARK
1	INTERNAL CHASSIS	96031-902-110	PC/ABS	-1-	
2	ASS'Y LCD/DIGITIZER	94985-102-810		-1-	
3	GASKET LCD	98704-905-310	NEOPRENE SPONGE	-2-	
4	ASS'Y LCD CONTROL B'D	99112-102-811		-1-	
5	CONTROL B'D HARNESS	93056-107-003		-1-	
6	SCREW	97002-120-601	FH+ M2.0*6 FE FZY	-1-	
7	SCREW	97008-126-051	BH+ M2.6*5 FE FZY	-1-	
	STYLUS-PEN	94992-100-003	UP-201-04A(WACOM)	-1-	
	BATTERY (ALK)	94719-102-820	6N-50AAA(SANYO)	-1-	
	UTILITY S/W MNL	99116-102-BLS	NOTEPAD1 UTIL LS	-1-	
	DISKETTE-ASS'Y	94091-500-200	MS-DOS 5.0A 3.5" SEC	-1-	
	FUSE	94709-903-020	TR5-T NO19374X(FM) F2	-1-	
	ADAPTER	94969-002-610	AD-26A(SEK)	-1-	

REV3. : 1992.07.02.(OHK)

EXPLODED VIEW (1/3)
NOTE-PAD

삼성전자주식회사

ASSEMBLY & DEASSEMBLY DRAWING (AC ADAPTER)



No	DESCRIPTION	SPEC	QTY
01	CASE-BOTTOM	PC+ABS,ALLOY	1
02	CASE,COVER	PC+ABS,ALLOY	1
03	PCB ASSY		1
04	LED PCB ASSY		1
05	HEAT-SINK 1		1
06	HEAT-SINK 2		1
07	TR-CLAMP		1
08	AC-INLET		1
09	RUBBER FOOT		4
10	LABEL	DESIGNATION	1
11	INSULATOR		1
12	INSULATOR		3
13	SCREW MACH		1
14	SCREW MACH		2
15	SCREW ITAPPING		3
16	SCREW ITAPPING		1
17	RING-INSULATOR	PE	2
18	WASHER-SPRING		2
19	NUT-HEX		2
20	LED		3
21	LED-CAP		1
22	PVC-INSULATOR	PVC	1
23	OUTPUT CABLE ASSY		1

Appendix C

Reference Material

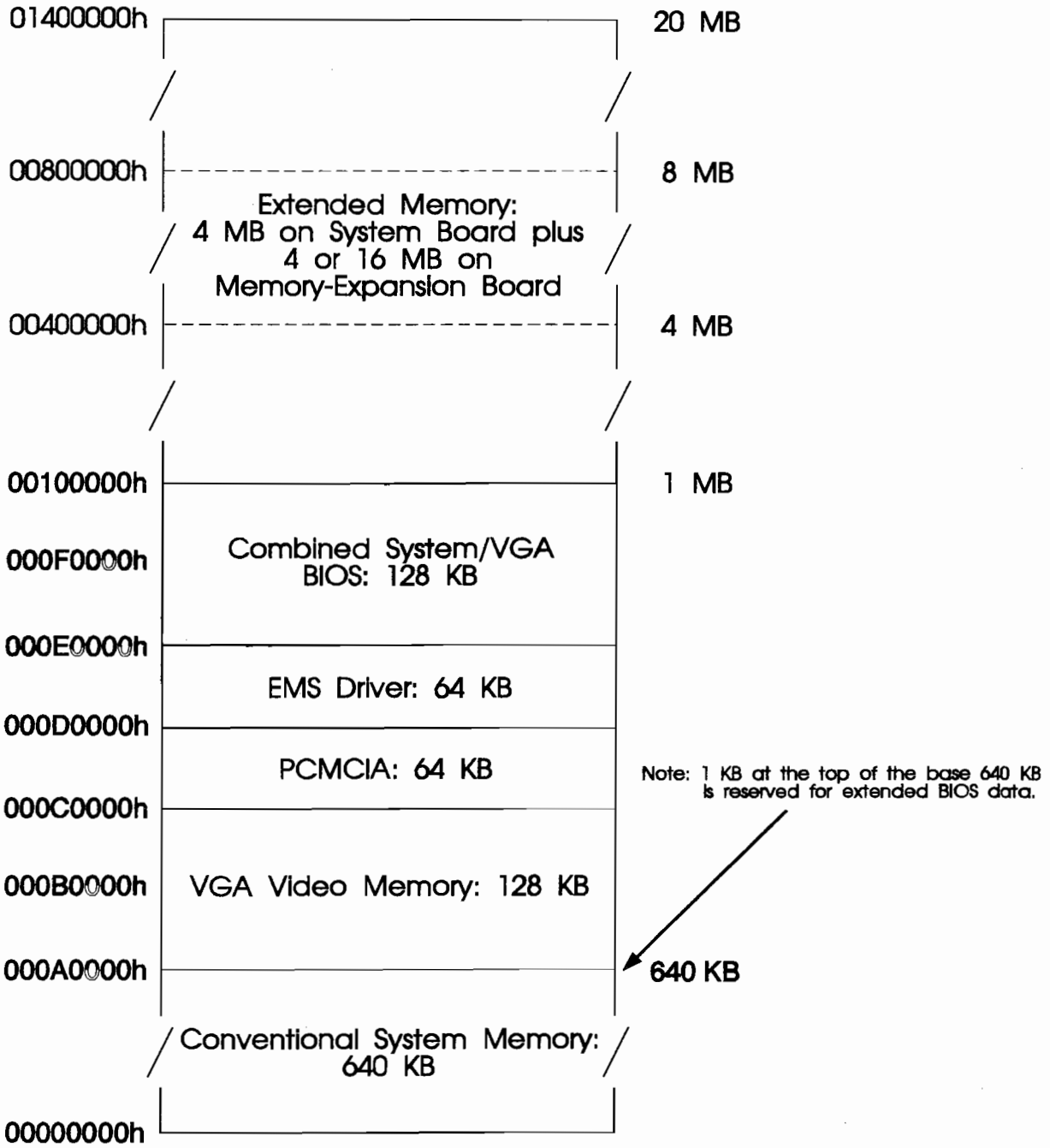
Hardware Interrupt (IRQ) Map

Interrupt	Function
IRQ0	System timer
IRQ1	Keyboard
IRQ2	Cascade interrupt
IRQ3	Serial port 2
IRQ4	Serial port 1
IRQ5	PCMCIA
IRQ6	Diskette drive controller
IRQ7	Parallel port 1
IRQ8	RTC
IRQ9	Redirect Int 0Ah (IRQ2 handler)/VGA
IRQ10	Digitizer
IRQ11	Global access
IRQ12	Mouse
IRQ13	Numeric coprocessor
IRQ14	Hard disk drive controller
IRQ15	Unused

I/O Map

Address	Device
000–01F	DMA controller 1, 8237A–5
020–03F	Interrupt controller 1, 8259A, Master
040–05F	Timer, 8254-2
060–06F	8042 (Keyboard)
070–07F	Real-time clock, NMI (non-maskable interrupt) mask
080–09F	DMA page register, 74LS612
0A0–0BF	Interrupt controller 2, 8259A
0C0–0DF	DMA controller 2, 8237A-5
0F0	Clear math coprocessor busy
0F1	Reset math coprocessor
0F8–0FF	Math coprocessor
1F0–1F8	Hard disk
218–21F	PCMCIA controller
220–223	Digitizer controller
278–27F	Parallel printer port 2
2F8–2FF	Serial port 2
378–37F	Parallel printer port 1
3B0–3BF	Monochrome display and printer adapter
3C0–3CF	Enhanced graphics adapter
3D0–3DF	Color graphics adapter
3F0–3F7	Diskette drive controller
3F8–3FF	Serial port 1

Memory Map


01400000h
20 MB
00800000h
8 MB
Extended Memory:
4 MB on System Board plus
4 or 16 MB on
Memory-Expansion Board
00400000h
4 MB
00100000h
1 MB
000F0000h
Combined System/VGA
BIOS: 128 KB
000E0000h
EMS Driver: 64 KB
000D0000h
PCMCIA: 64 KB
000C0000h
000B0000h
VGA Video Memory: 128 KB
000A0000h
640 KB
Conventional System Memory:
640 KB
00000000h
Note: 1 KB at the top of the base 640 KB
is reserved for extended BIOS data.

Acronym List

A	ampere: unit of electrical current flow
ABS	acrylonitrile-butadiene-styrene
AC	alternating current
ASCII	American Standard Code for Information Interchange
ASIC	application-specific integrated circuit
ASL	above sea level
AT	Advanced Technology (from the IBM AT model computer)
BIOS	basic input/output system
BPI	bits per inch
BPS	bits per second
CCFT	cold-cathode flourescent tube
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
DIN	Deutsche Industrie Normenausschuss (German standard-setting association – used to refer to the type of connector used for keyboard and mouse interfaces)
DRAM	dynamic random-access memory
EMS	Expanded Memory Specification
EPROM	erasable programmable read-only memory
FDC	floppy disk (diskette drive) controller
FDD	floppy disk (diskette) drive
FSTN	film super-twisted nematic
HDC	hard disk controller
HDD	hard disk drive
Hz	Hertz: unit of electrical frequency (formerly cps, or cycles per second)
IC	integrated circuit
IDE	integrated drive electronics
I/O	input/output

ISA	industry standard architecture
JEIDA	Japananese Electronic Industry Development Association
Kb	kilobit: 1024 bits
KB	kilobyte: 1024 bytes
LCD	liquid-crystal display
LED	light-emitting diode
mA	milliampere: 1/1000 of an ampere
MB	megabyte: 1,048,576 bytes
MHz	megahertz: 1,000,000 cycles per second
ms	millisecond: 1/1000 of a second
NiCd	nickel cadmium
ns	nanosecond: 1/1,000,000,000 of a second
PCBA	printed circuit board assembly
PC	personal computer
PC	polycarbonate
PCMCIA	Personal Computer Memory Card International Association
PLCC	plastic-leaded chip carrier (chip package)
POST	power-on self test
RAM	random-access memory
RFI	radio-frequency interference
ROM	read-only memory
RPM	revolutions per minute
RTC	real-time clock
SRAM	static random-access memory
TPI	tracks per inch
V	volt: unit of electro-motive force
VAC	volts, alternating current
VDC	volts, direct current

VRAM	video RAM
VGA	video graphics array
W	watt: unit of electrical power
Whr	watt hour: unit of stored electrical power
XMS	eXpanded Memory Specification
XT	eXtended Technology (from the IBM XT model computer)

Units of Measurement

µ	micro: 1/1,000,000 multiplier
µs	microsecond: 1/1,000,000 of a second
A	ampere: unit of electrical current flow
B	byte
b	bit
bpi	bits per inch
bps	bits per second
Hz	Hertz: unit of electrical frequency (formerly cps, or cycles per second)
K	kilo: times 1024 (used with binary terms)
k	kilo: times 1000 (used with non-binary terms)
KB	kilobyte: 1024 bytes
Kb	kilobit: 1024 bits
M	mega: times 1,048,576 when used with binary terms; times 1,000,000 (used with non-binary terms)
mA	milliampere: 1/1000 of an ampere
MHz	megahertz: 1,000,000 cycles per second
ms	millisecond: 1/1000 of a second
MB	megabyte: 1,048,576 bytes
n	nano: 1/1,000,000,000 multiplier
ns	nanosecond: 1/1,000,000,000 of a second
rpm	revolutions per minute
TPI	tracks per inch
V	volt: unit of electro-motive force
W	watt: unit of electrical power
Whr	watt hour: unit of stored electrical power

98134-375-099
Rev. 1.0
Printed in Korea